

Compal Confidential

GH4FZ Schematics Document

AMD Cezanne (FP6) Platform
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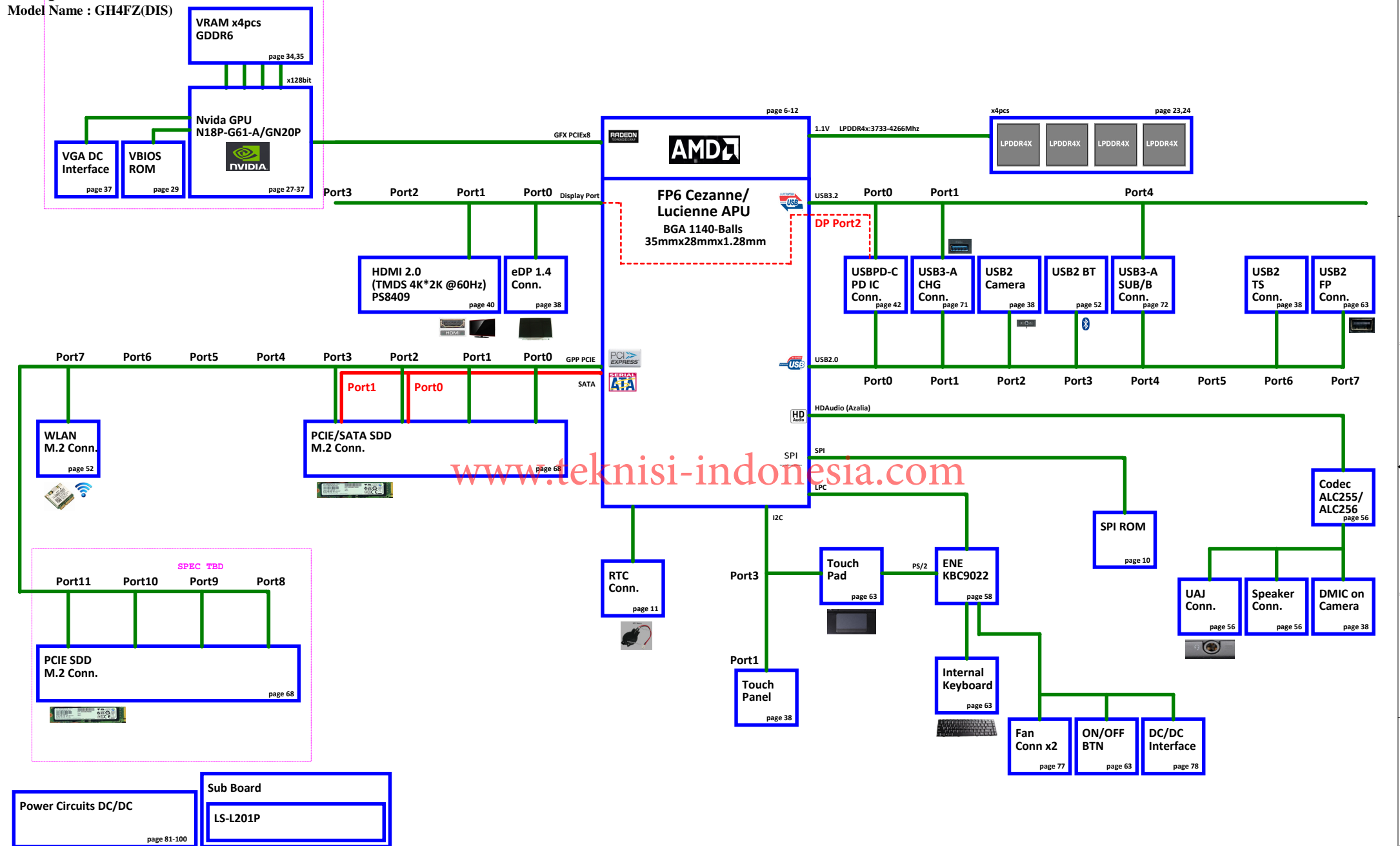
LA-L202P REV:1.0

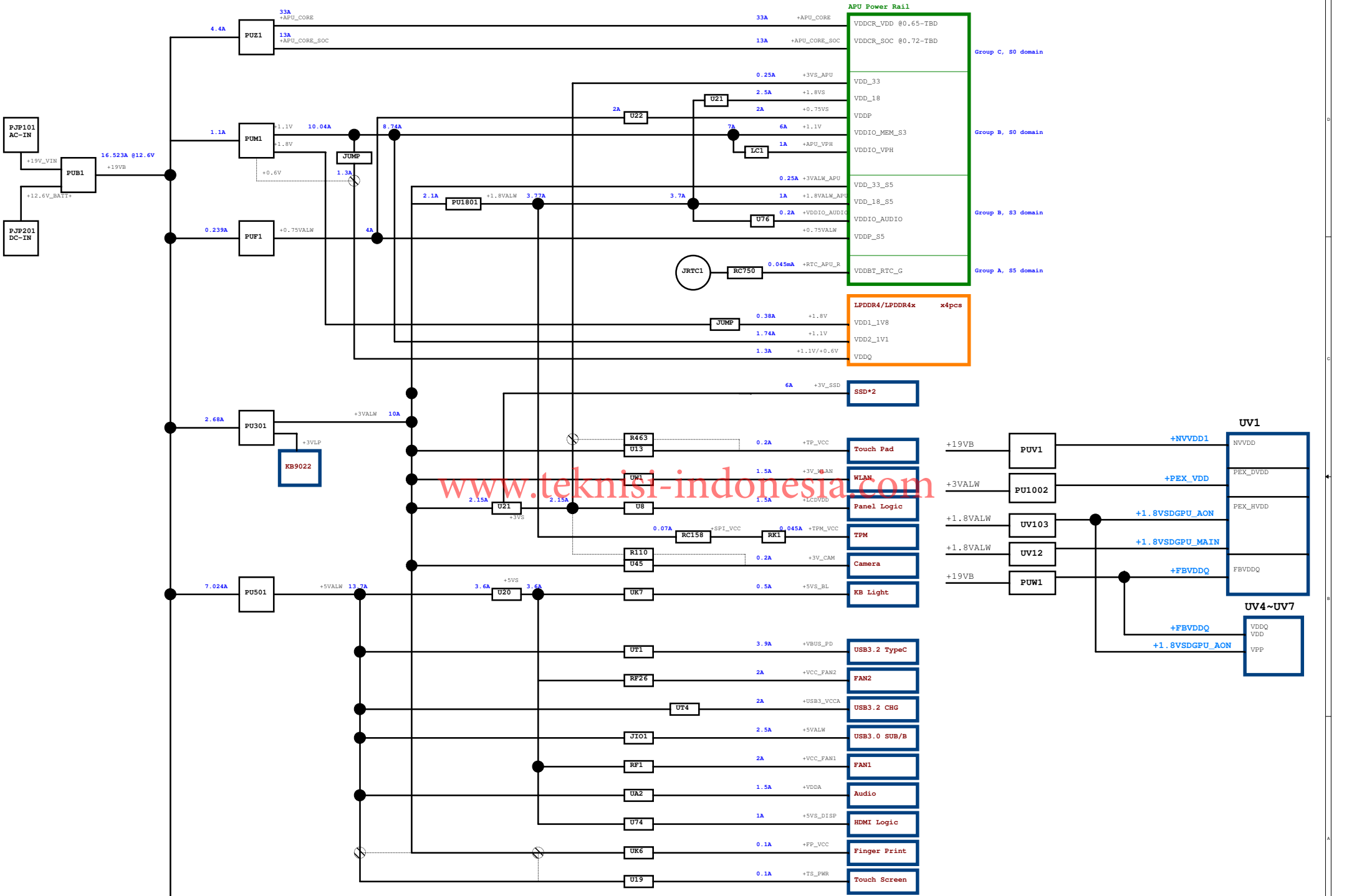
2021-04-08

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Date: Wednesday, May 05, 2021				Sheet	1	of 102

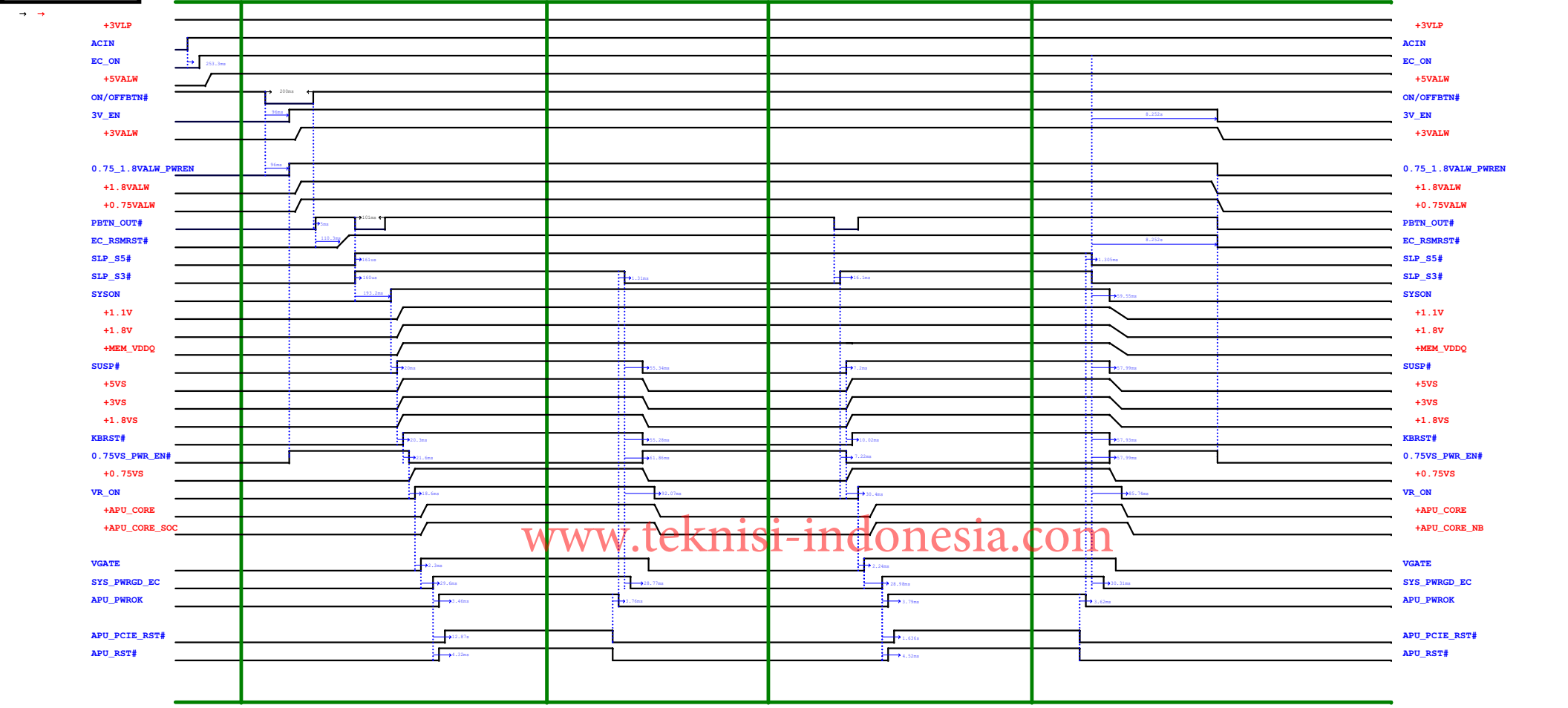
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Model Name : GH4FZ(DIS)



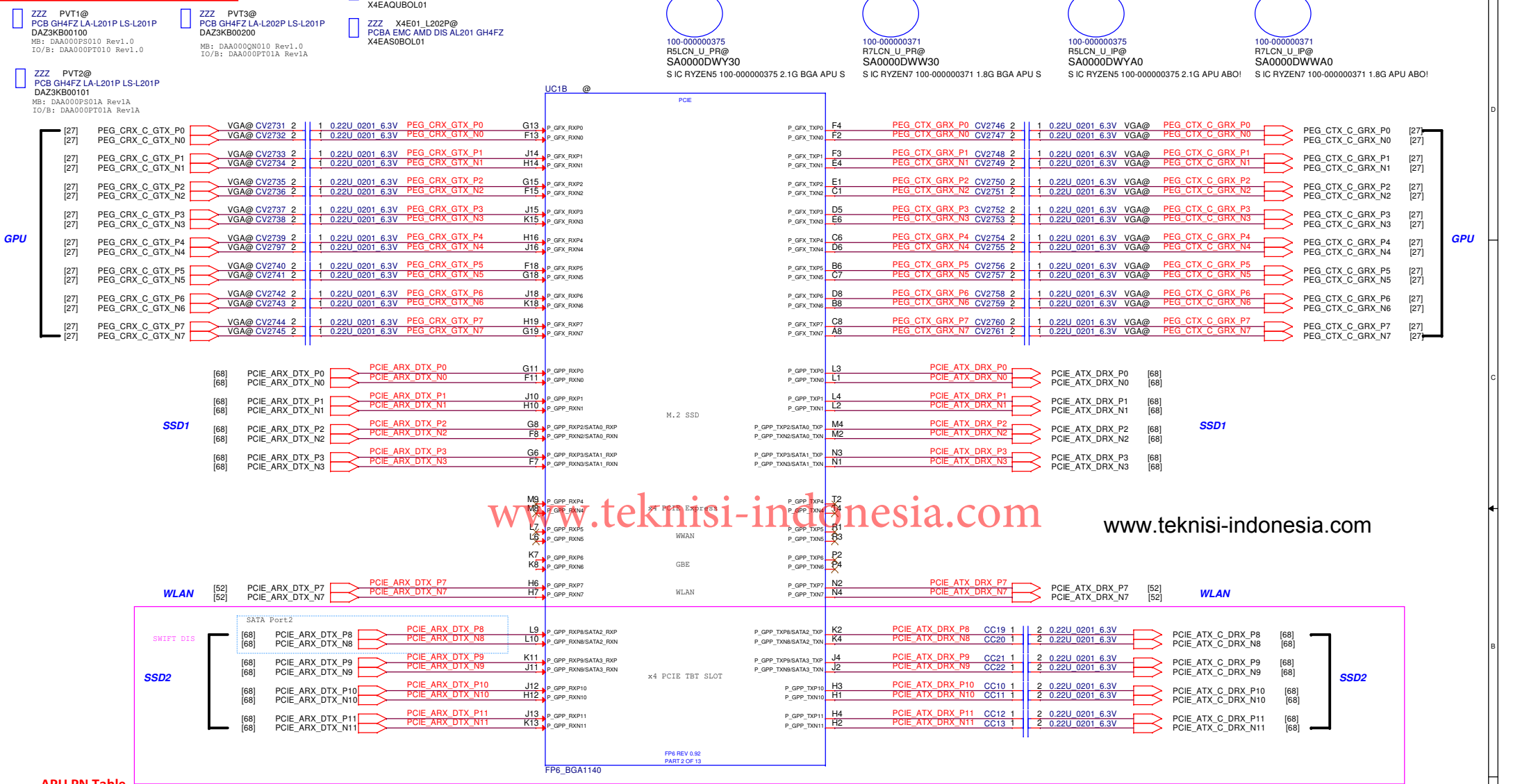


Power Sequence



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Main Func = CPU



APU PN Table

APU Platform	Customer PN	Cezanne	Customer PN	Cezanne	Customer PN	Cezanne	Customer PN	Cezanne	Customer PN	Lucienne	Customer PN	Lucienne	Customer PN	Lucienne
Renoir	UC1	100-000000287-40 R5CZS_U_PC@ SA0000E1000	UC1	100-000000285-40 R7CZS_U_IP@ SA0000DWS10	UC1	100-000000295-40 R5CZS_H_PC@ SA0000E1P00	UC1	100-000000300-40 R7CZS_H_PC@ SA0000E1N00	UC1	100-000000376-40 R7LCN_U_PC@ SA0000DWW00	UC1	100-000000375-40 R7LCN_U_PC@ SA0000DWWY00	UC1	100-000000371-40 R7LCN_U_IP@ SA0000DWWV00
		S IC RYZEN5 100-000000287-40 2.1G APU S		S IC RYZEN7 100-000000285-40 1.8G APU S		S IC RYZEN 100-000000295-40 3G BGA APU S		S IC RYZEN 100-000000300-40 3.1G APU S		S IC RYZEN 100-000000376-40 2.6G APU S		S IC RYZEN 100-000000375-40 2.1G BGA S		S IC RYZEN 100-000000371-40 1.8G APU S

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Title

FP6 (1/7) PEG/PCIE/SATA

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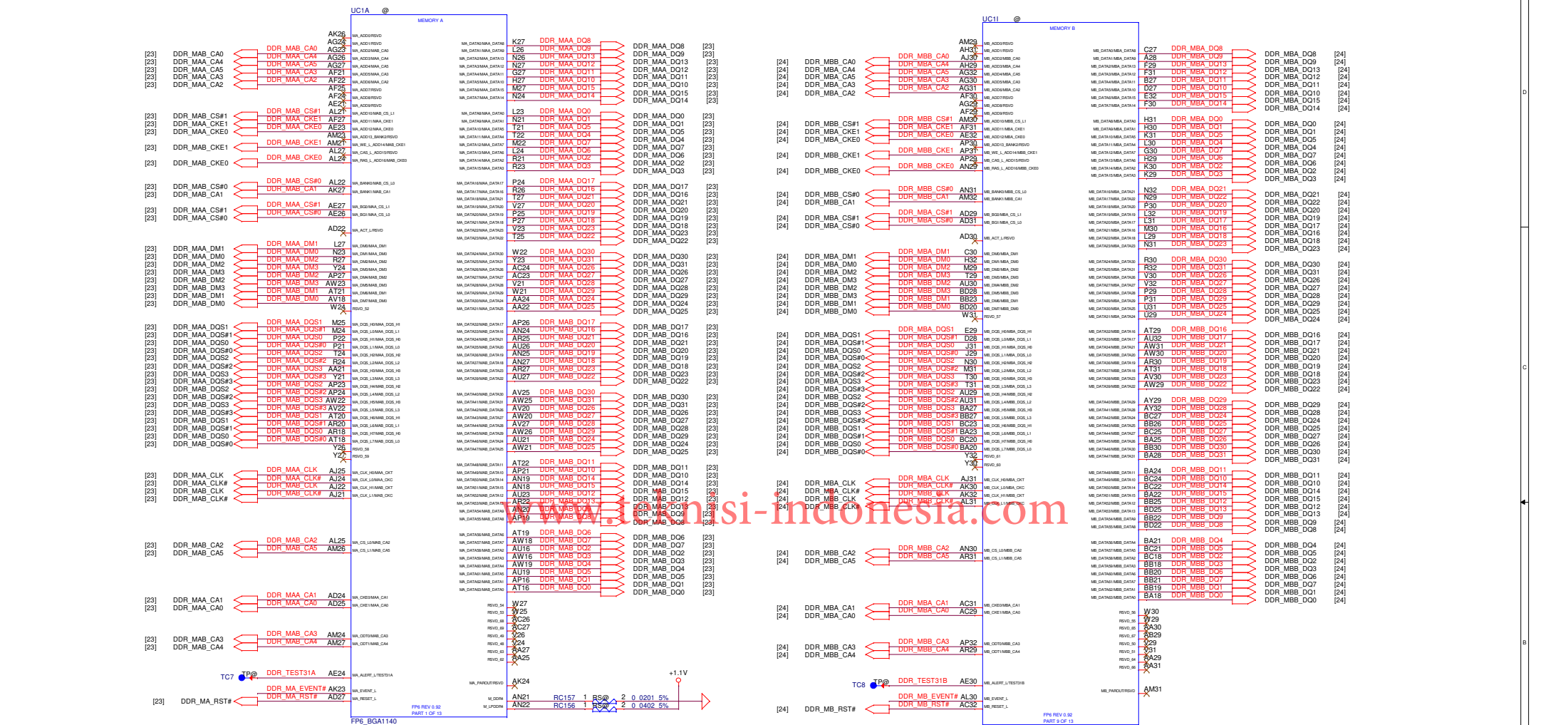
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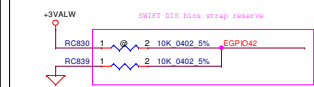
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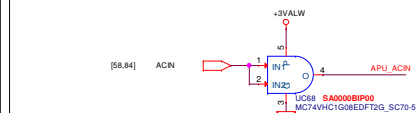
Main Func = CPU



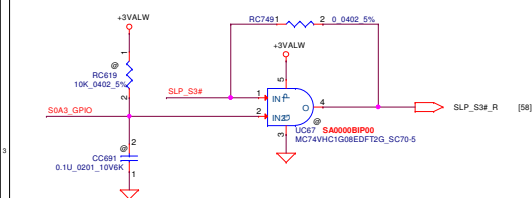
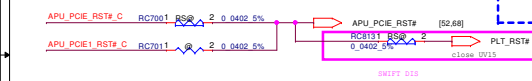
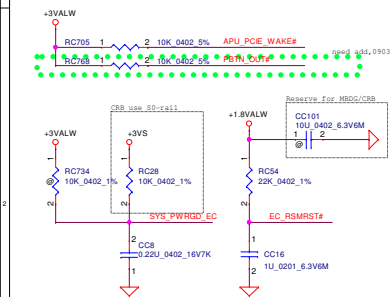
12C_1_SCL (62P/G147)	12C_1_SDA (62P/G148)	Project ID
H	Reserve	GH40Z (UMA)
L	Reserve	GH4FZ (DIS)



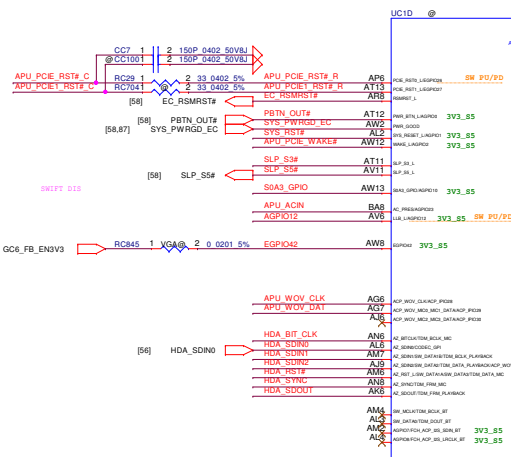
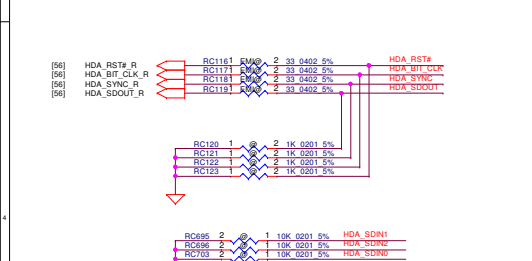
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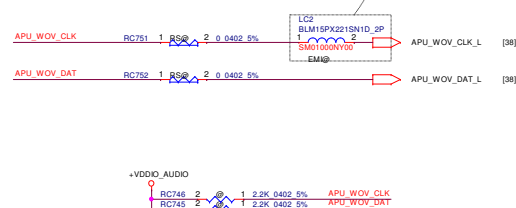
ACPI



HDA

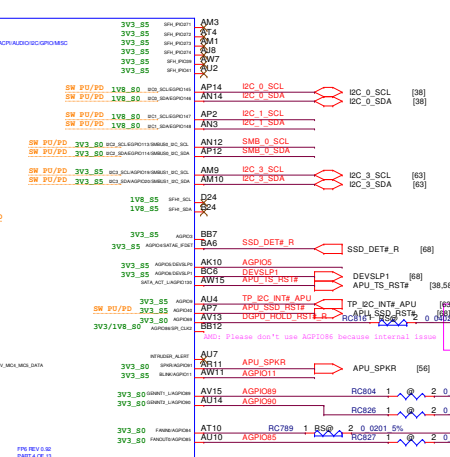
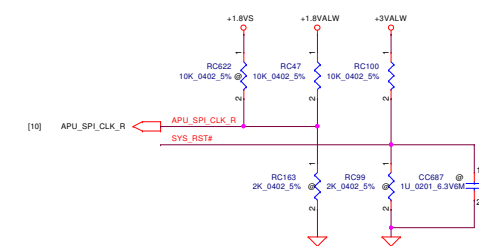


APU WOV



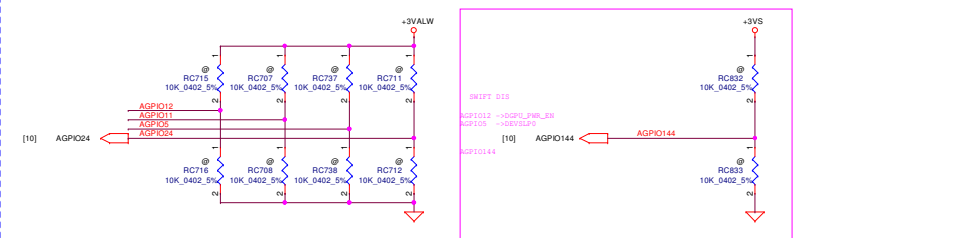
Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 4MHz CRYSTAL CLOCK	NORMAL RESET MODE (Default)
L	USE 100MHz PCIE CLOCK AS REFERENCE CLOCK	SHORT RESET MODE

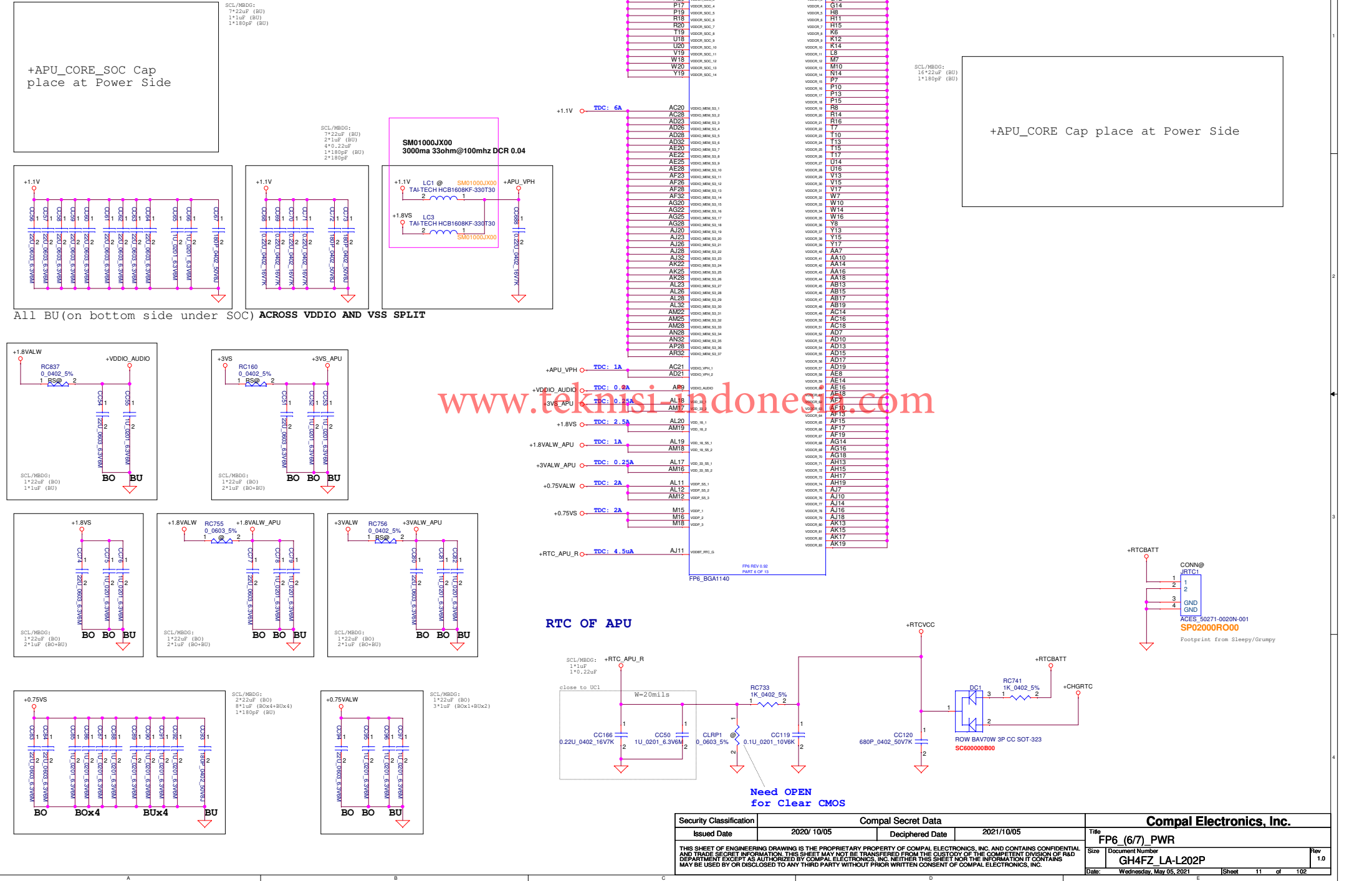


GPIO Table

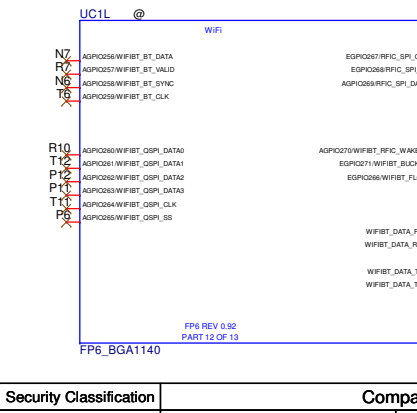
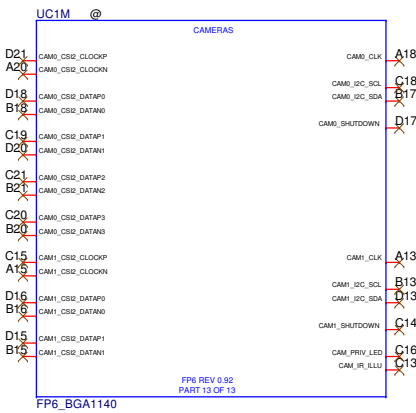
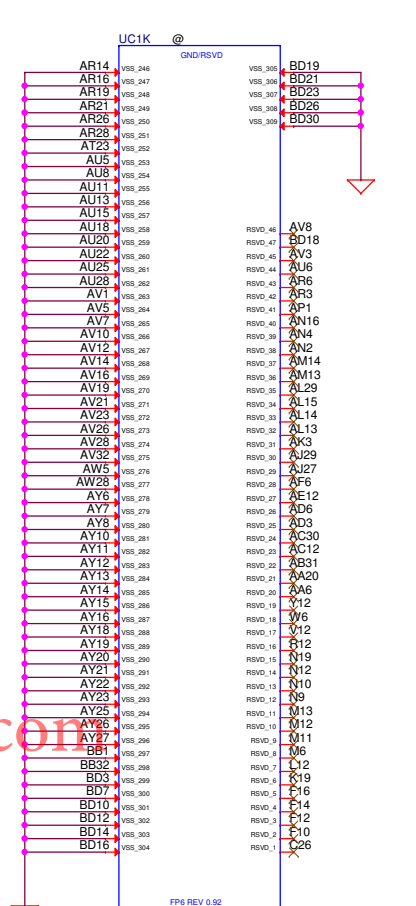
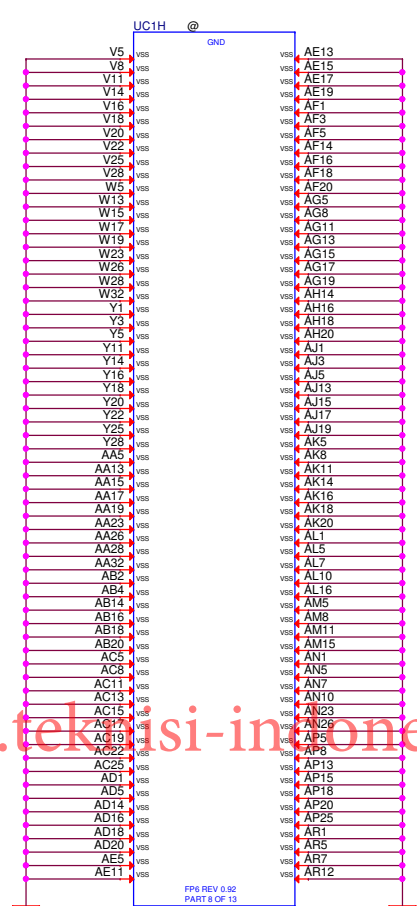
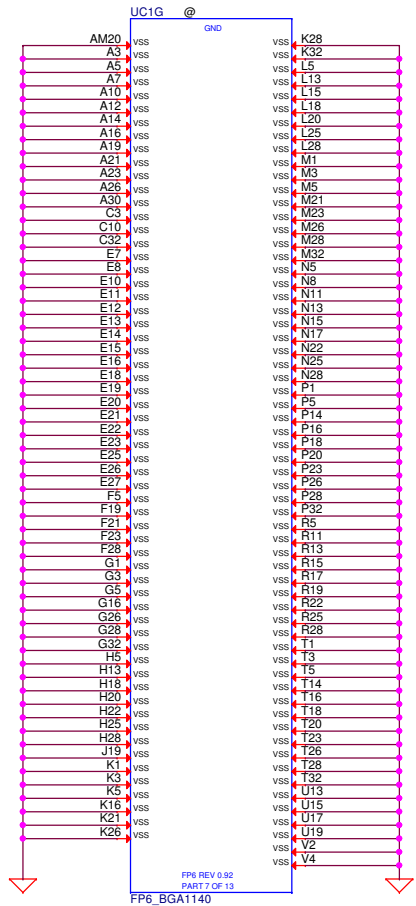
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0 0 0 1	SAM4_8GB J01 SAM4X 8GB@ SAM4X 8GB@ SAM4X 8GB@ SAM4X 8GB@ SA0000D9710 J02 S IC D4 16GB436 K4U8E354AA-MGCR ABO I
0 0 1 0	HYN4_8GB J01 HYN4X 8GB@ HYN4X 8GB@ HYN4X 8GB@ HYN4X 8GB@ SA0000DG010 J02 S IC D4 16GB436 HHCNNHNNKMLXN-NEE ABO I
0 0 1 1	MIC4X_16GB J01 MIC4X 16GB@ MIC4X 16GB@ MIC4X 16GB@ MIC4X 16GB@ SA0000D4030 J02 S IC D4 1033 MT33E1G32DNP-044 WT-A ABO I
0 1 0 0	SAM4X_16GB J01 SAM4X 16GB@ SAM4X 16GB@ SAM4X 16GB@ SAM4X 16GB@ SA0000D9810 J02 S IC D4 32G426 K4U8E3D4AA-MGCR ABO I
0 1 0 1	HYN4X_16GB J01 HYN4X 16GB@ HYN4X 16GB@ HYN4X 16GB@ HYN4X 16GB@ SA0000DG010 J02 S IC D4 32G426 HHCNNHNNKMLXN-NEE ABO I
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
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1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	



Main Func = CPU



Main Func = CPU



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				Date:	Wednesday, May 05, 2021
				Sheet	13 of 102
				Rev	1.0

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	14 of 102
				Rev	1.0

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				Date:	Wednesday, May 05, 2021
				Sheet	15 of 102
				Rev	1.0

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	16 of 102
				Rev	1.0

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				Date:	Wednesday, May 05, 2021
				Sheet	17 of 102
				Rev	1.0

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				Date:	Wednesday, May 05, 2021
				Sheet	18 of 102
				Rev	1.0

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				Date:	Wednesday, May 05, 2021
				Sheet	19 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	20 of 102
				Rev	1.0

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				Date:	Wednesday, May 05, 2021
				Sheet	21 of 102
				Rev	1.0

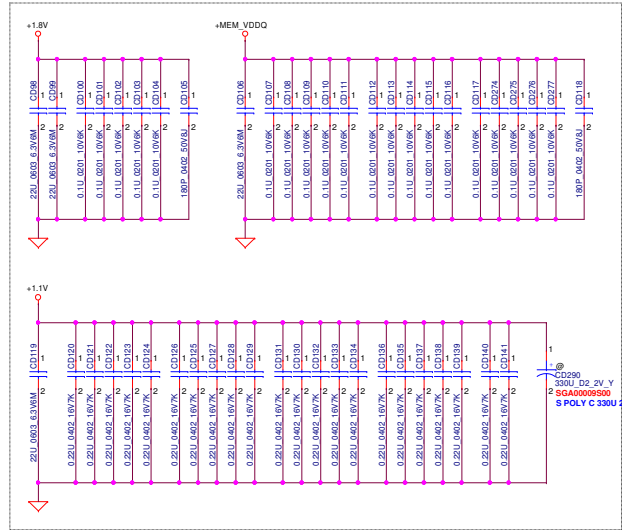
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				Date:	Wednesday, May 05, 2021
				Sheet	22 of 102
				Rev	1.0

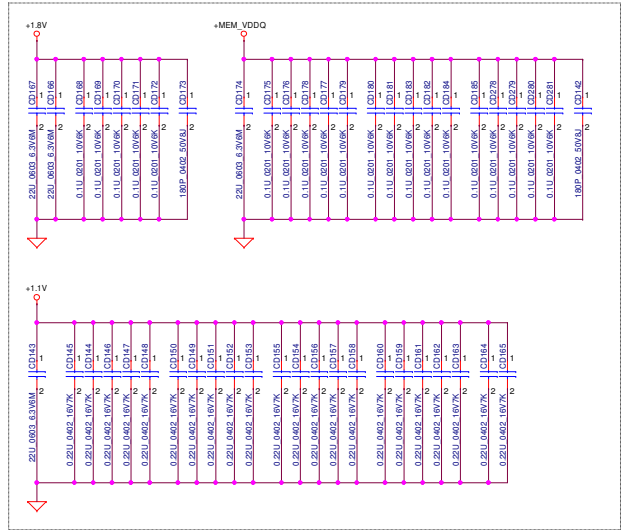


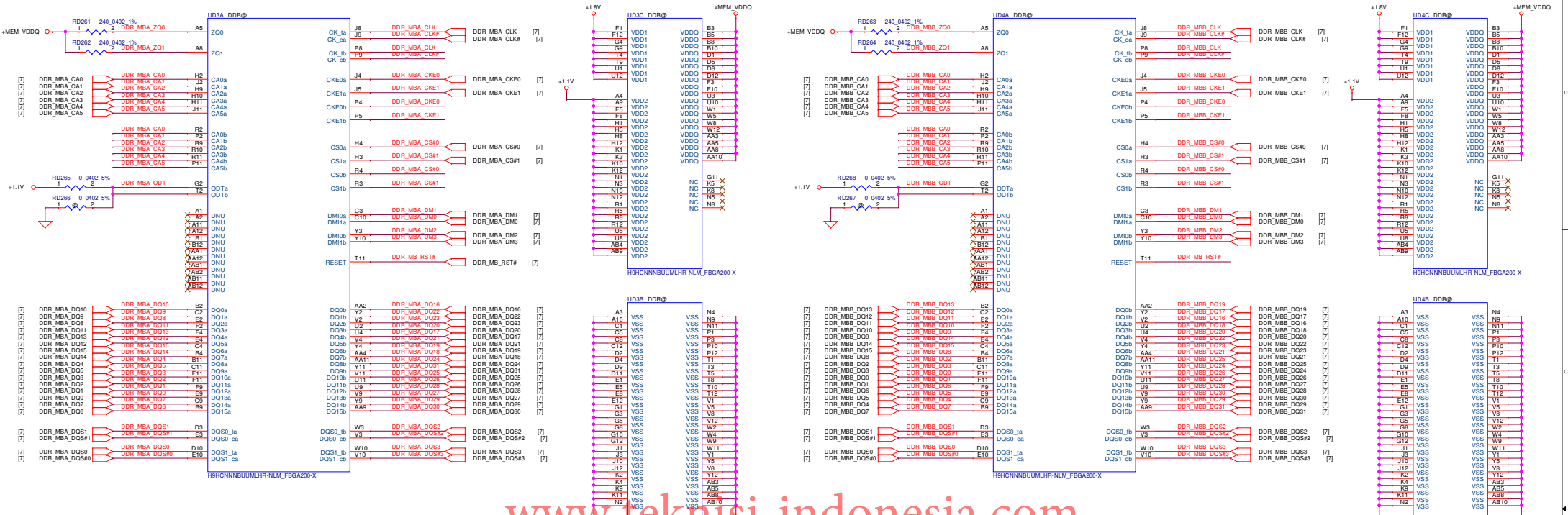
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For UD1



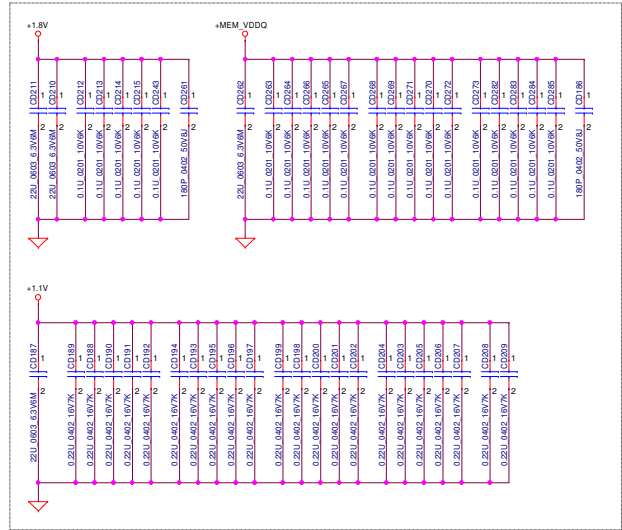
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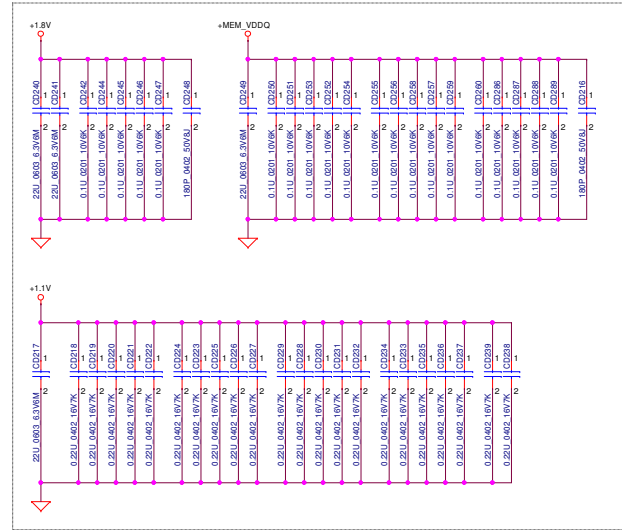


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For UD3



For UD4



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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	25 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	26 of 102
				Rev	1.0

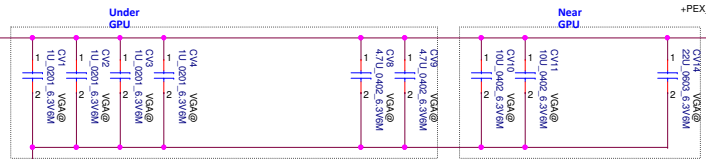
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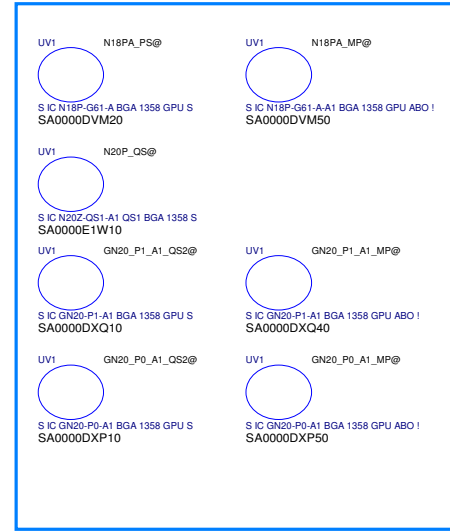
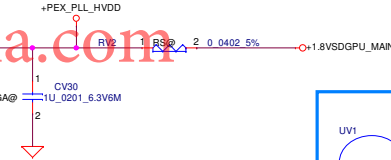
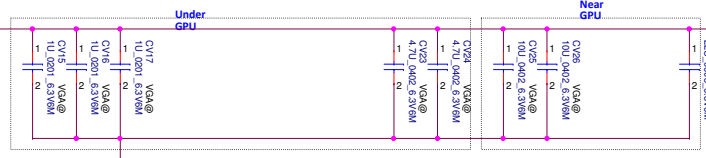
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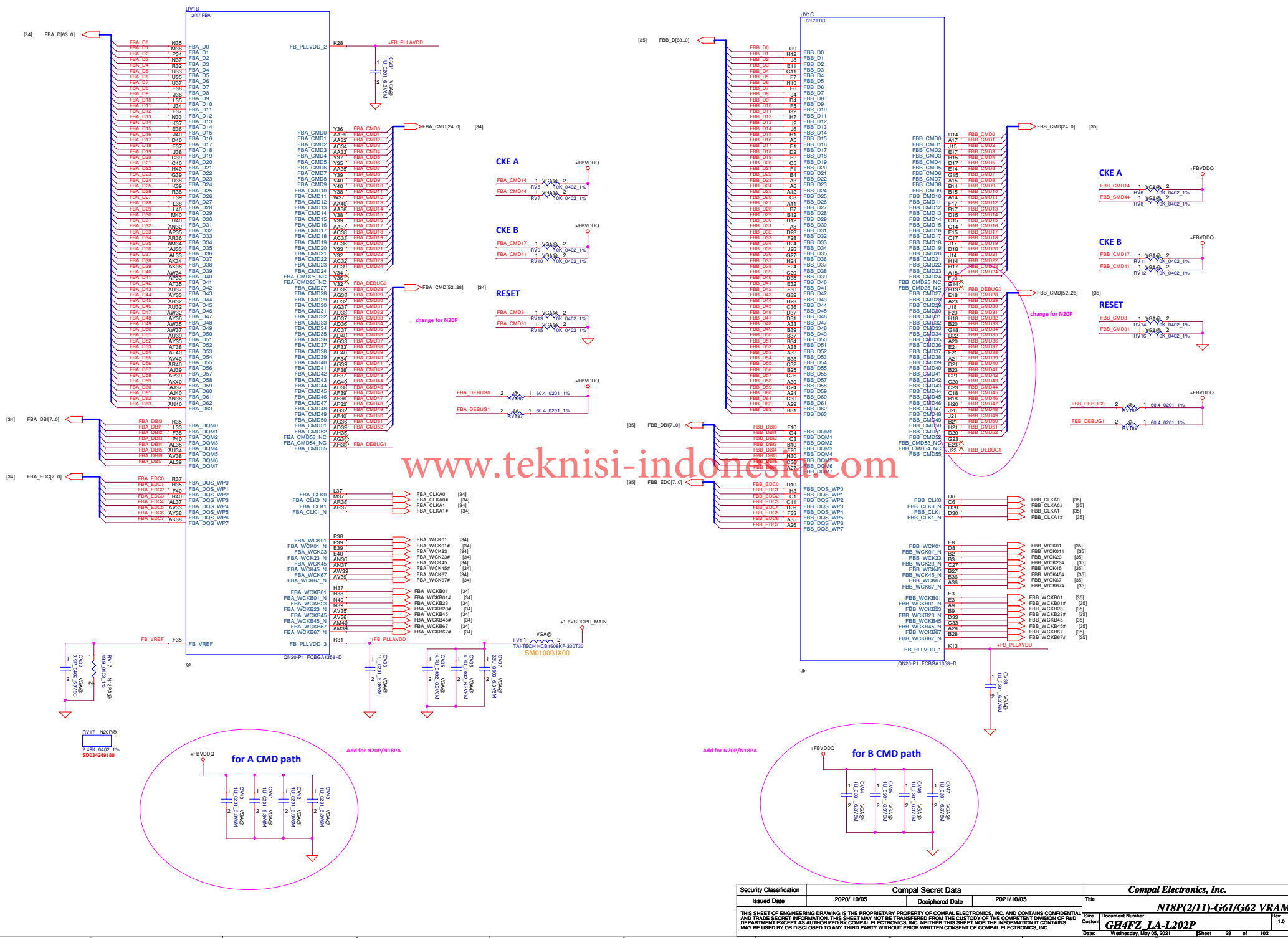


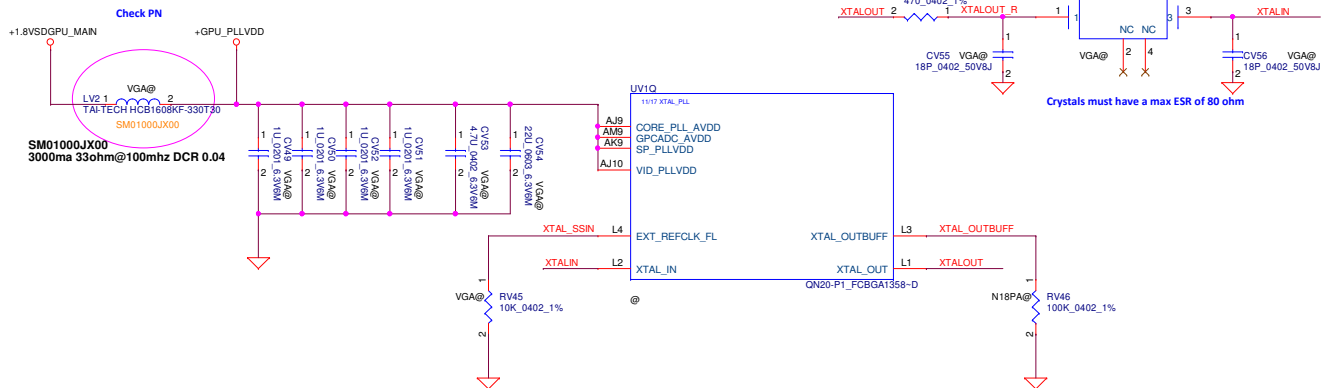
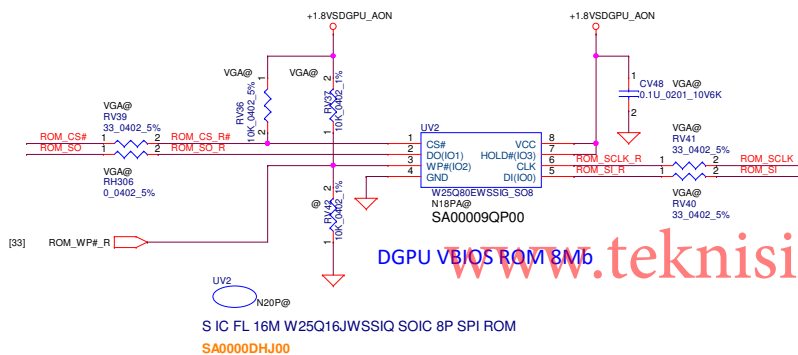
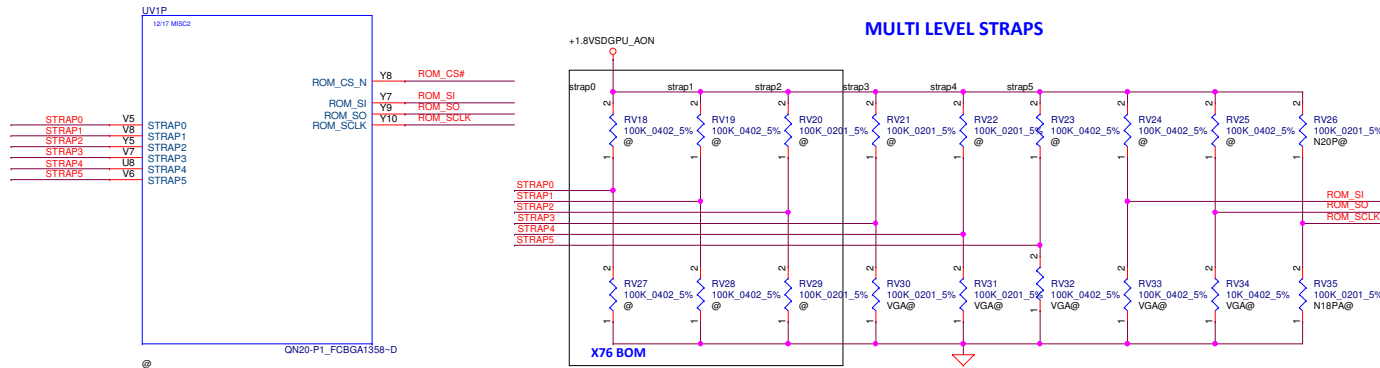
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		Custom		GH4FZ_LA-L202P		1.0		Sheet		27 of 102	

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N18P-G61-A

Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)

Table 11.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

ROM_SO	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	L	L	L	L	RVL	RVL	RVL

SAMSUNG (000)	VSA4G@	RV27 100K_0402_5%	SD028100380	VSA4G@	RV28 100K_0402_5%	SD028100380	VSA4G@	RV29 100K_0201_5%	SD043100380	ZZZ	VRAM N18 Micron4GB
MICRON (001)	VMIC4G@	RV18 100K_0402_5%	SD028100380	VMIC4G@	RV28 100K_0402_5%	SD028100380	VMIC4G@	RV29 100K_0201_5%	SD043100380	ZZZ	VRAM N18 Samsung4GB
HYNIX (010)	VHYN4G@	RV27 100K_0402_5%	SD028100380	VHYN4G@	RV19 100K_0402_5%	SD028100380	VHYN4G@	RV29 100K_0201_5%	SD043100380	ZZZ	VRAM G20 Micron4GB
											VRAM G20 Samsung4GB
											VRAM G20 Hynix4GB
											VRAM G20 Hynix4GB

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)

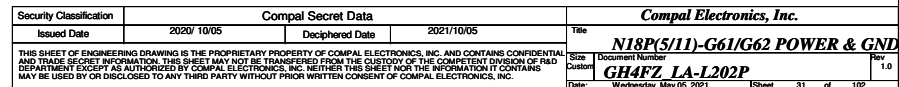
Table 9.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

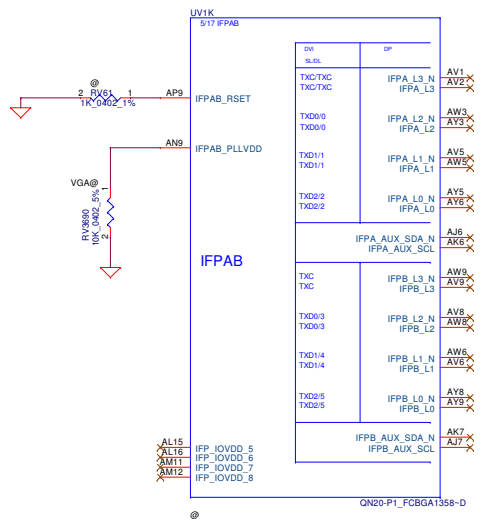
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

ROM_SO (10K)	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	H	L	L	H	RVL	RVL	RVL

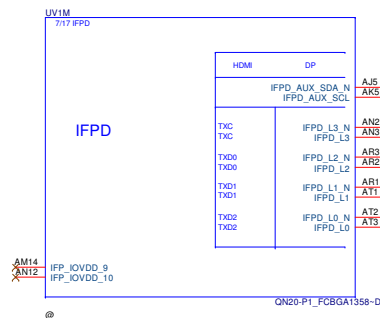
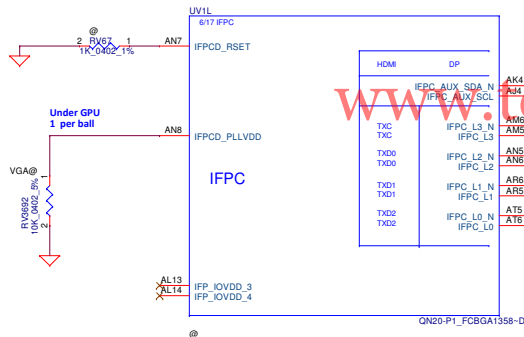
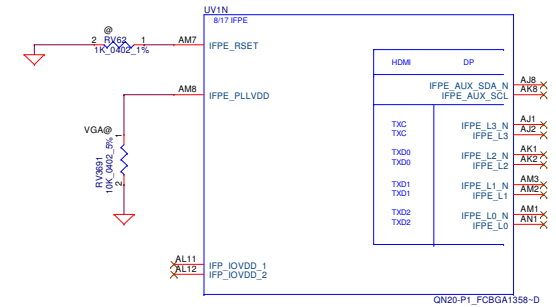
ROM_SO	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	H	L	L	L	RVL	RVL	RVL

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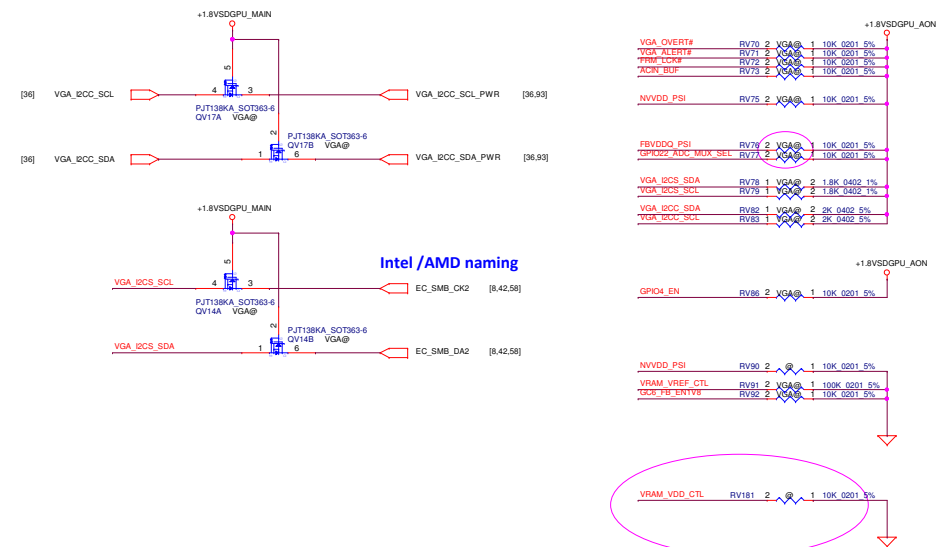


Check layout for port connection.

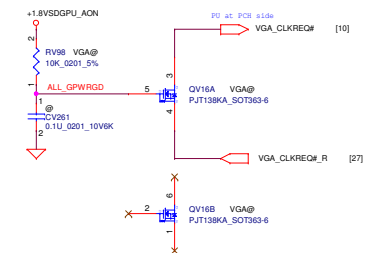


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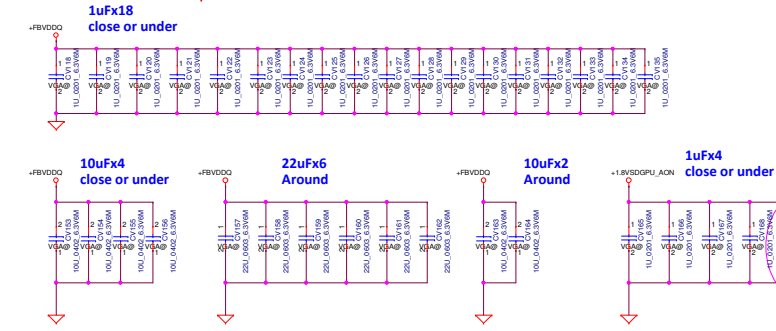
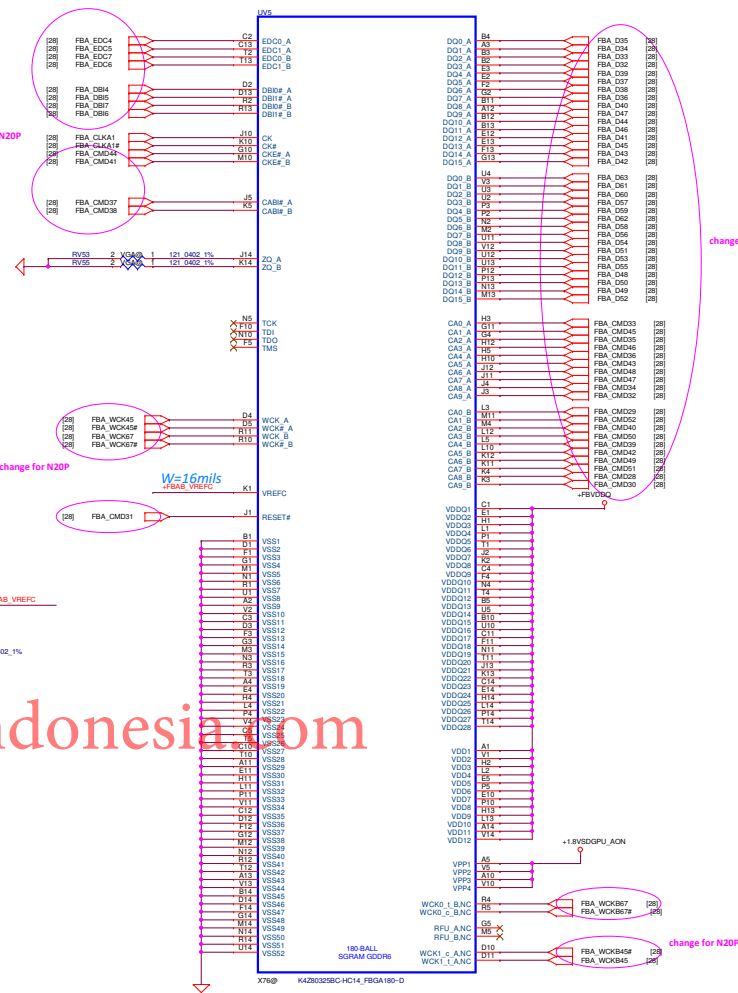
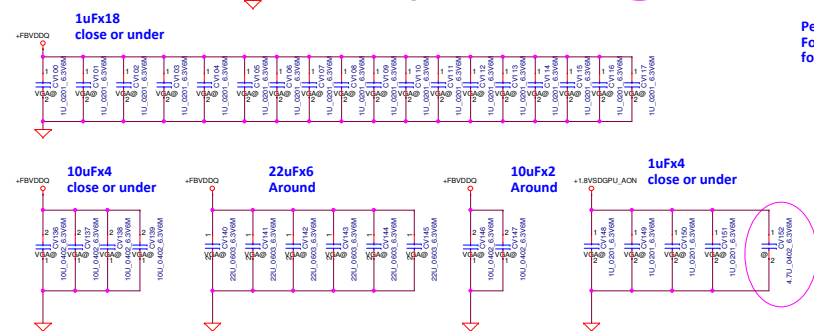
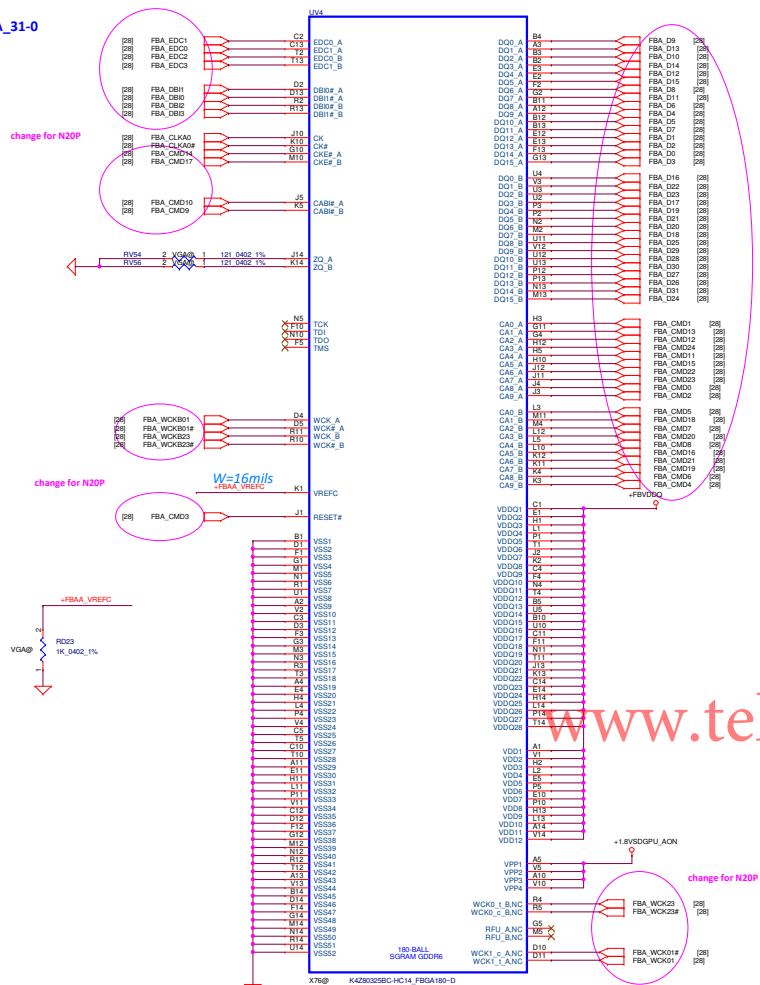
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			Date: Wednesday, May 05, 2021	
			Sheet	33 of 102



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GEN2 gain control by VBIO5

RV101 GEN2@
0_0402 5%
SD028000080

RV106 GEN2@
0_0402 5%
SD028000080

NV Suggest

For OVRM Keep ON

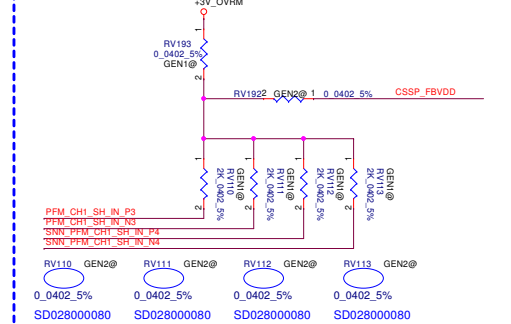
GEN2 gain control by VBIO5

RV103 GEN2@
0_0402 5%
SD028000080

RV109 GEN2@
0_0402 5%
SD028000080

GEN2 NV suggest BS_IN3,4 need also connect with BS_IN2 (CSSP_FBVDD)

No use SH_P/N need PD the same voltage as no use BS_IN



PFM CH1 SH IN P3
PFM CH1 SH IN N3
SNN PFM CH1 SH IN P4
SNN PFM CH1 SH IN N4

RV110 GEN2@
0_0402 5%
SD028000080

RV111 GEN2@
0_0402 5%
SD028000080

RV112 GEN2@
0_0402 5%
SD028000080

RV113 GEN2@
0_0402 5%
SD028000080

NV Suggest no use IMON PIN
uPI PD GND
ON NC Floating

NV Suggest reserve and not pop

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UV10 ON_GEN2@
S IC NCP4545XMTWGFN 32P MONITOR
SA0000DUX00

UV10 uPI_GEN2@
S IC US5651AQI WQFN 32P POWER MONITOR
SA0000DY100

UV10 uPI_GEN1@
S IC US5650QKI WQFN 32P POWER MONITOR
SA0000CMA00

RV104 uPI_GEN1@
487 0402 1%
SD00000EL80

RV122 uPI_GEN1@
357 0402 1%
SD034357080

RV132 uPI_GEN1@
324K 0402 1%
SD034324380

RV108 uPI_GEN1@
487 0402 1%
SD00000EL80

RV123 uPI_GEN1@
357 0402 1%
SD034357080

ADSRO (Pin21) ADSR1 (Pin22, PFM_CM_REF_IN)

ON-SEMI Suggest need add RC filter.

Pin23 : I2C_CLK (PFM_BG_REF_OUT)
Pin24 : I2C_DATA (PFM_BS_REF)

Follow NV CRB, OVRM/PWR IC use same I2C power rail.

OVRM Type

ZZZ X76N18G1_UP1@ N18_Gen1 uPI X76907BO061

ZZZ X76N18G1_ON N18_Gen1 ON X76907BO062

ZZZ X76GN20G1_UP1@ GN20_Gen1 uPI X76907BO069

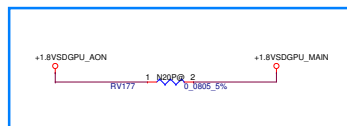
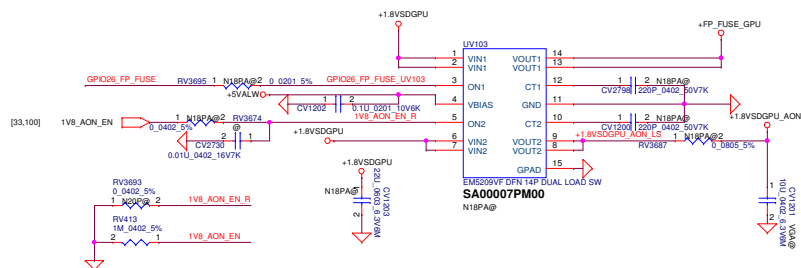
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ZZZ X76GN20G2_UP1@ GN20_Gen2 uPI X76907BO063

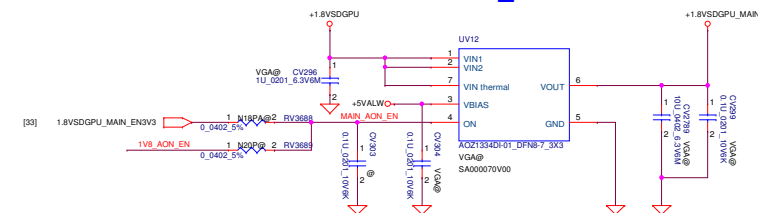
ZZZ X76GN20G2_ON GN20_Gen2 ON X76907BO064

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				N18P(10/11)-G61/G62 OVR-M	
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				Sheet 36 of 102	

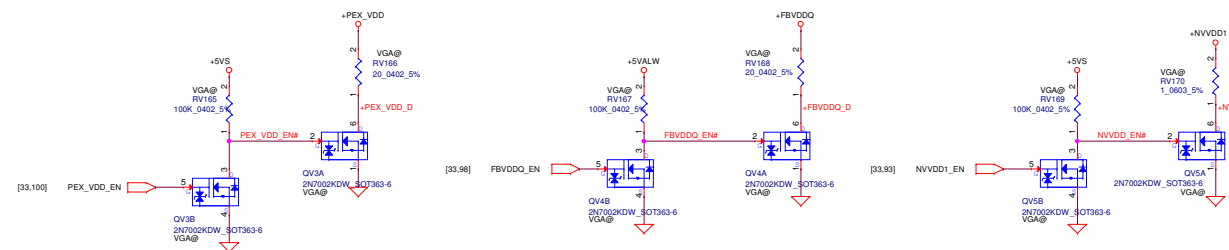
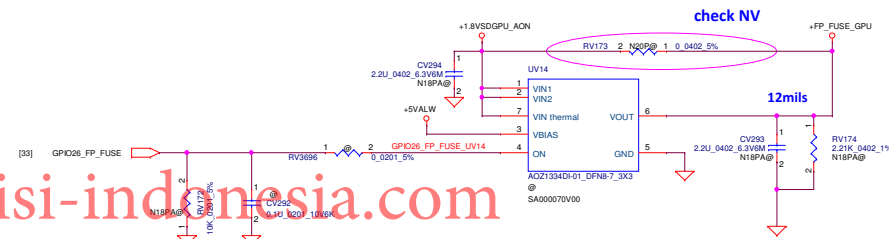
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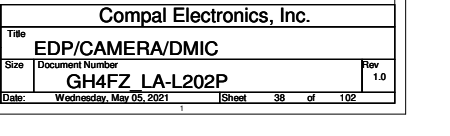
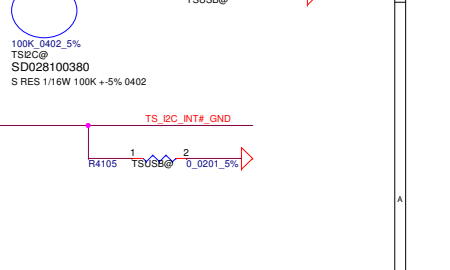
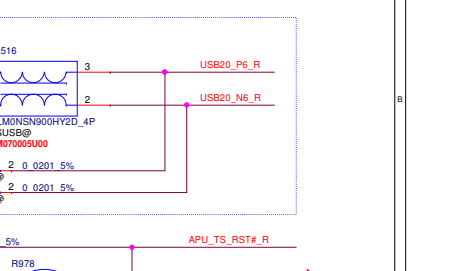
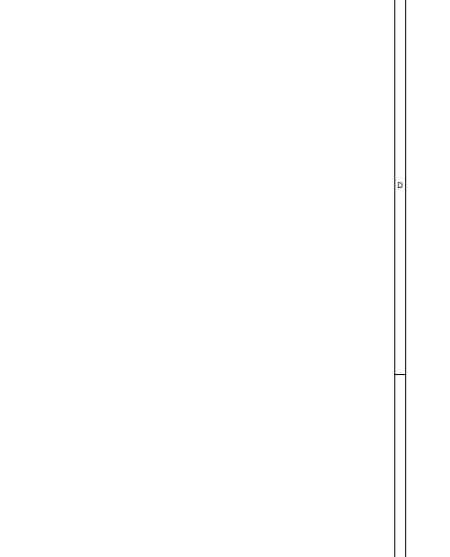
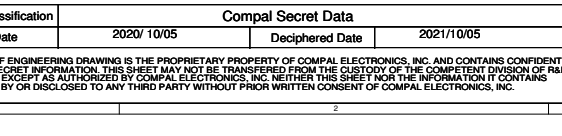
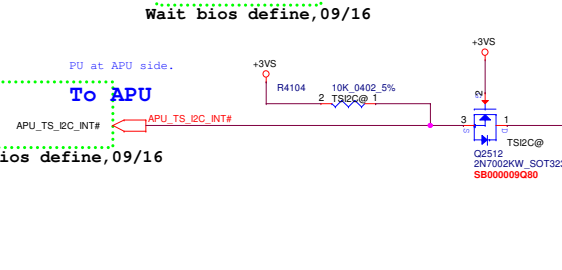
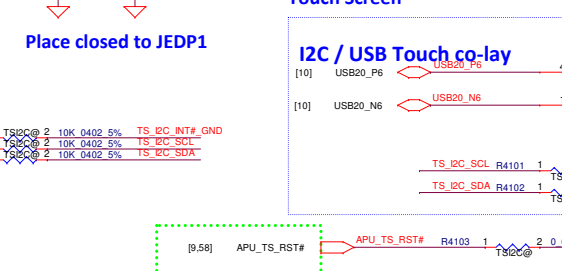
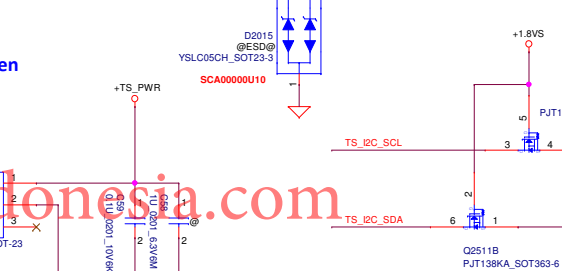
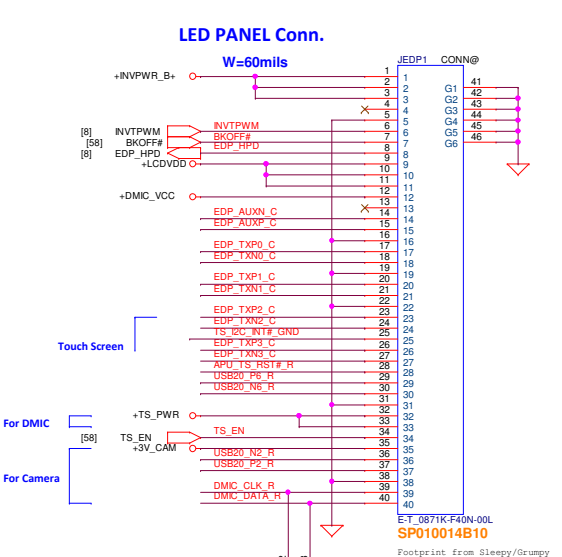
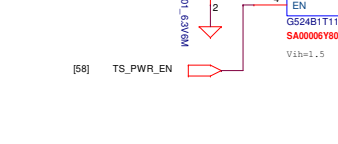
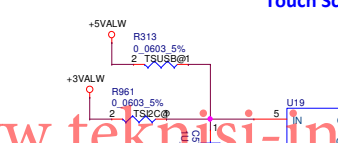
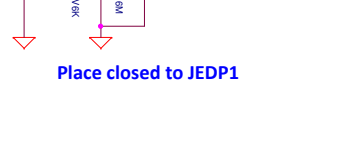
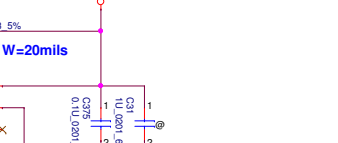
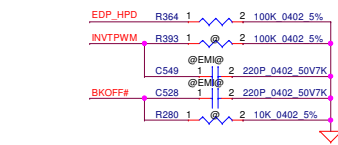
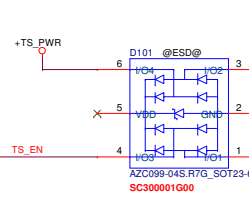
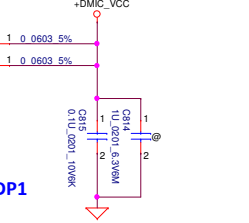
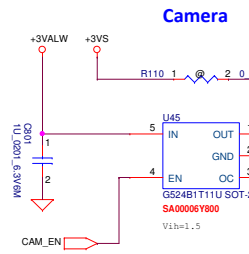
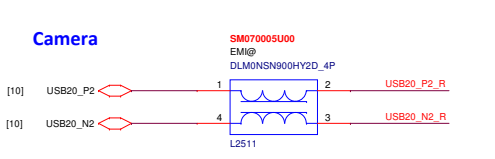
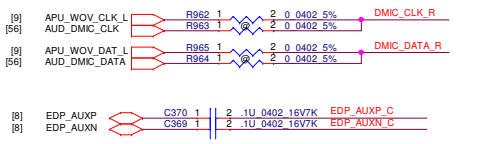
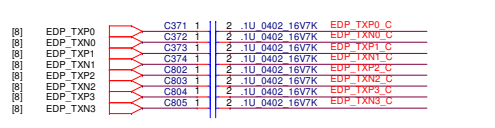
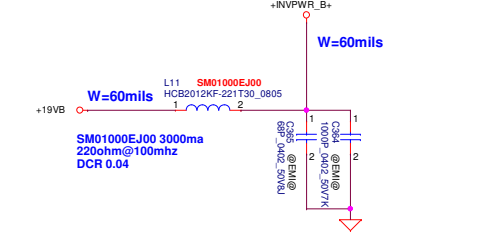
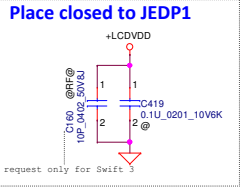
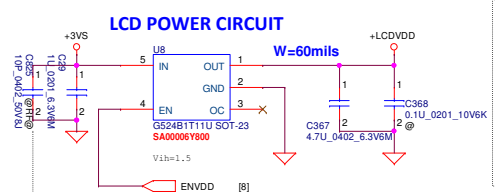


+1.8V_MAIN



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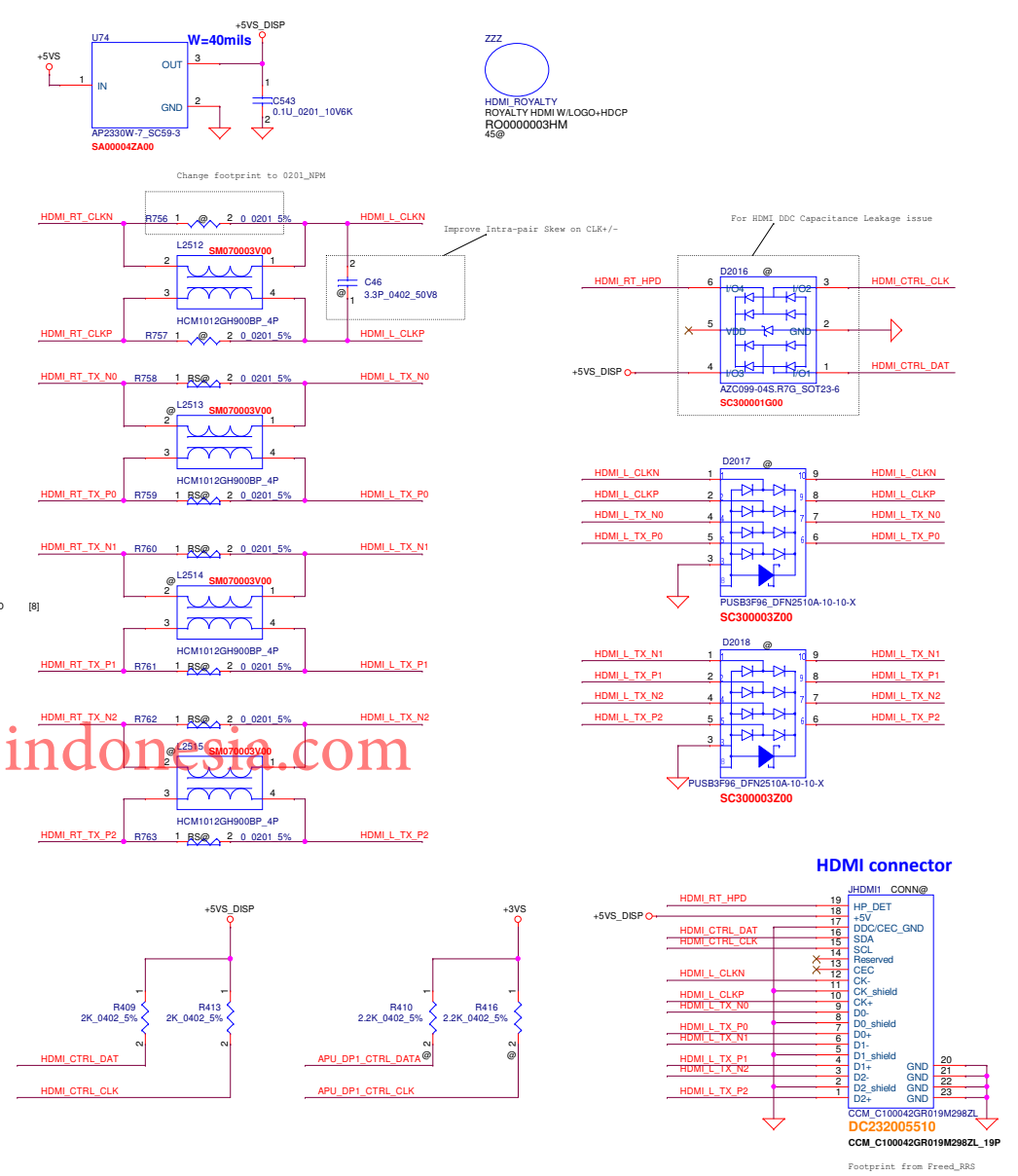
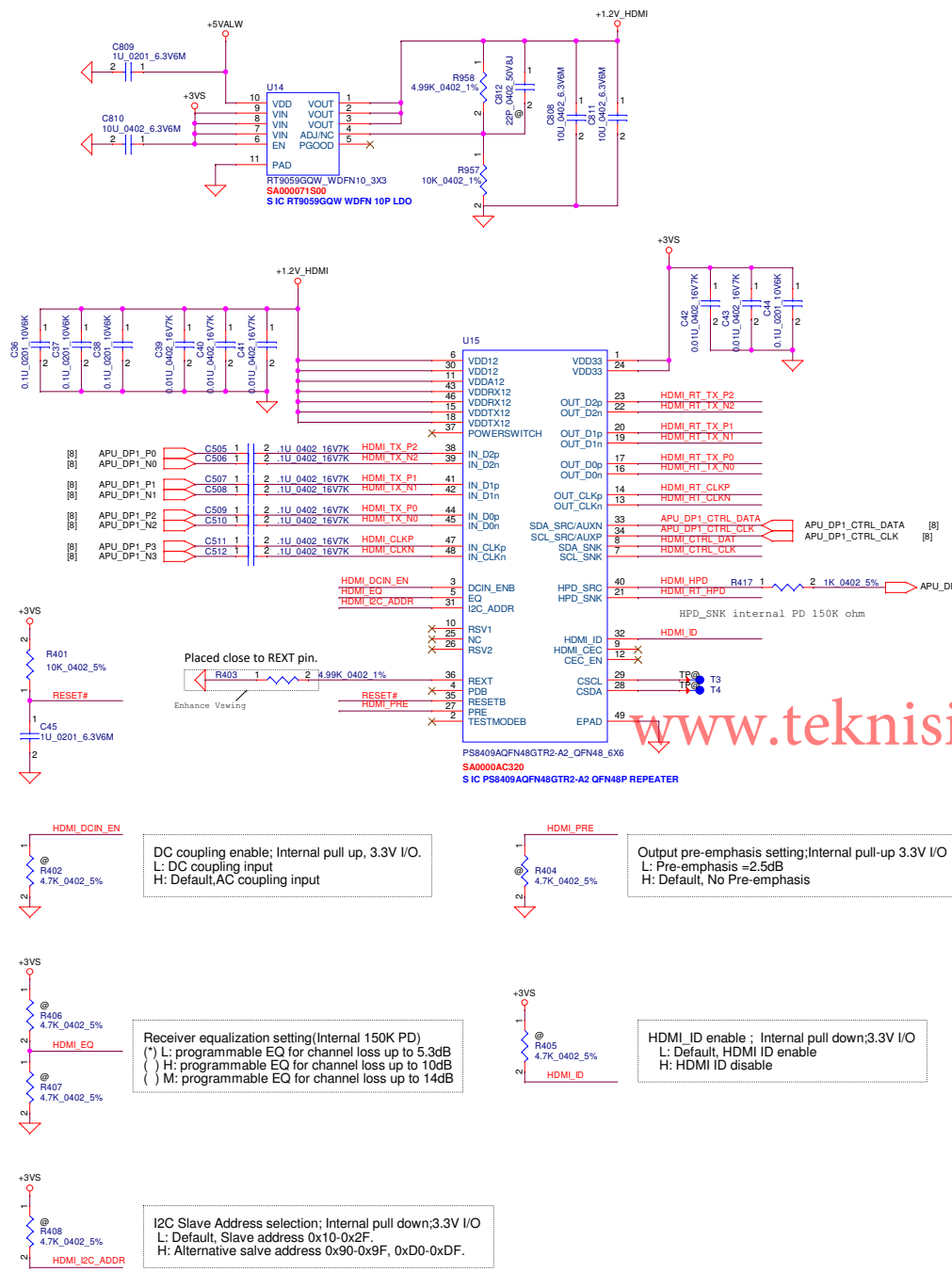


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				Date	Wednesday, May 05, 2021
				Sheet	38 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	39 of 102
				Rev	1.0

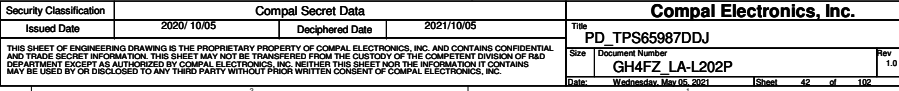


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								Customer		GH4FZ_LA-L202P				1.0	
								Date		Wednesday, May 05, 2021				Sheet	
														40 of 102	

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	41 of 102
				Rev	1.0



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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	43 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	44 of 102
				Rev	1.0

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	45 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	46 of 102
				Rev	1.0

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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	47 of 102
				Rev	1.0

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	48 of 102
				Rev	1.0

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	49 of 102
				Rev	1.0

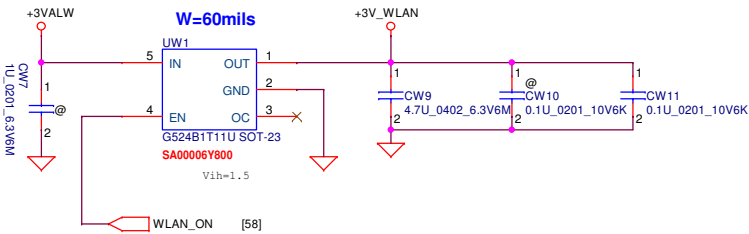
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	50 of 102
				Rev	1.0

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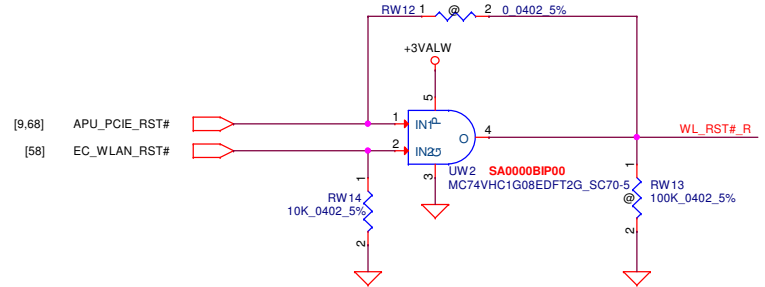
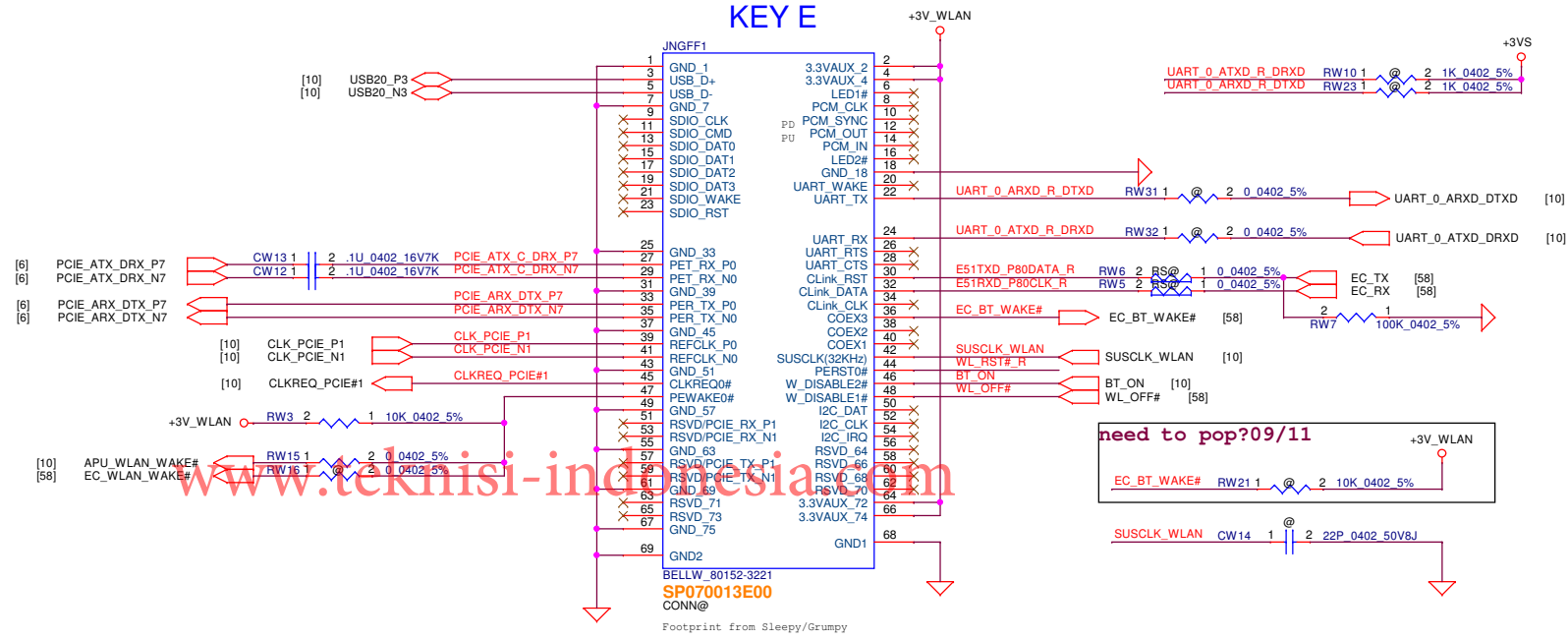
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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	51 of 102
				Rev	1.0

Wireless LAN



NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC(GPIO)/PEWake#	RESERVED/REFCLKP1	71
68	UIM_Power_SINK/CLKREQ#	GND	69
66	UIM_SWP/PERST#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O)(3.3)	GND	63
60	IQCC CLK (O)(0.3.3)	Reserved/PETn1	61
58	IQCC DATA (I/O)(0.3.3)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(0.3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0.3.3V)	PEWake# (O)(0.3.3V)	55
52	PERST# (O)(0.3.3V)	CLKREQ# (O)(0.3.3V)	53
50	SUSCLK(32KHz) (O)(0.3.3V)	GND	51
48	CODEX1 (I/O)(0.1.8V)	REFCLKN0	49
46	CODEX20(O)(0.1.8V)	REFCLKP0	47
44	CODEX30(O)(0.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0.1.8V)	PETn0	37
34	UART CTS (I/O)(0.1.8V)	PETp0	35
32	UART Tx (O)(0.1.8V)	GND	33
<div></div>			23
22	UART Rx (I/O)(1.8V)	SDIO Reset# (O)(0.1.8V)	21
20	UART Wake# (I/O)(3.3V)	SDIO Wake# (I/O)(1.8V)	19
18	GND	SDIO DAT0(O)(0.1.8V)	17
16	LED#2 (I/CO)	SDIO DAT1(O)(0.1.8V)	15
14	PCM_OUT/IS_SD_OUT (O)(0.1.8V)	SDIO DAT2(O)(0.1.8V)	13
12	PCM_IN/IS_SD_IN (I/O)(1.8V)	SDIO DAT0(O)(0.1.8V)	11
10	PCM_SYNC/IS_VS (O)(0.1.8V)	SDIO CMD(O)(0.1.8V)	9
8	PCM_CLK/IS_SCK (O)(0.1.8V)	SDIO CLK(O)(0.1.8V)	7
6	LED#1 (I/CO)	GND	5
4	3.3V	USB_D-	3
2	3.3V	GND	1



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				Date:	Wednesday, May 05, 2021
				Sheet	53 of 102
				Rev	1.0

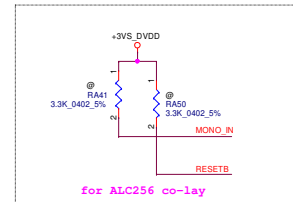
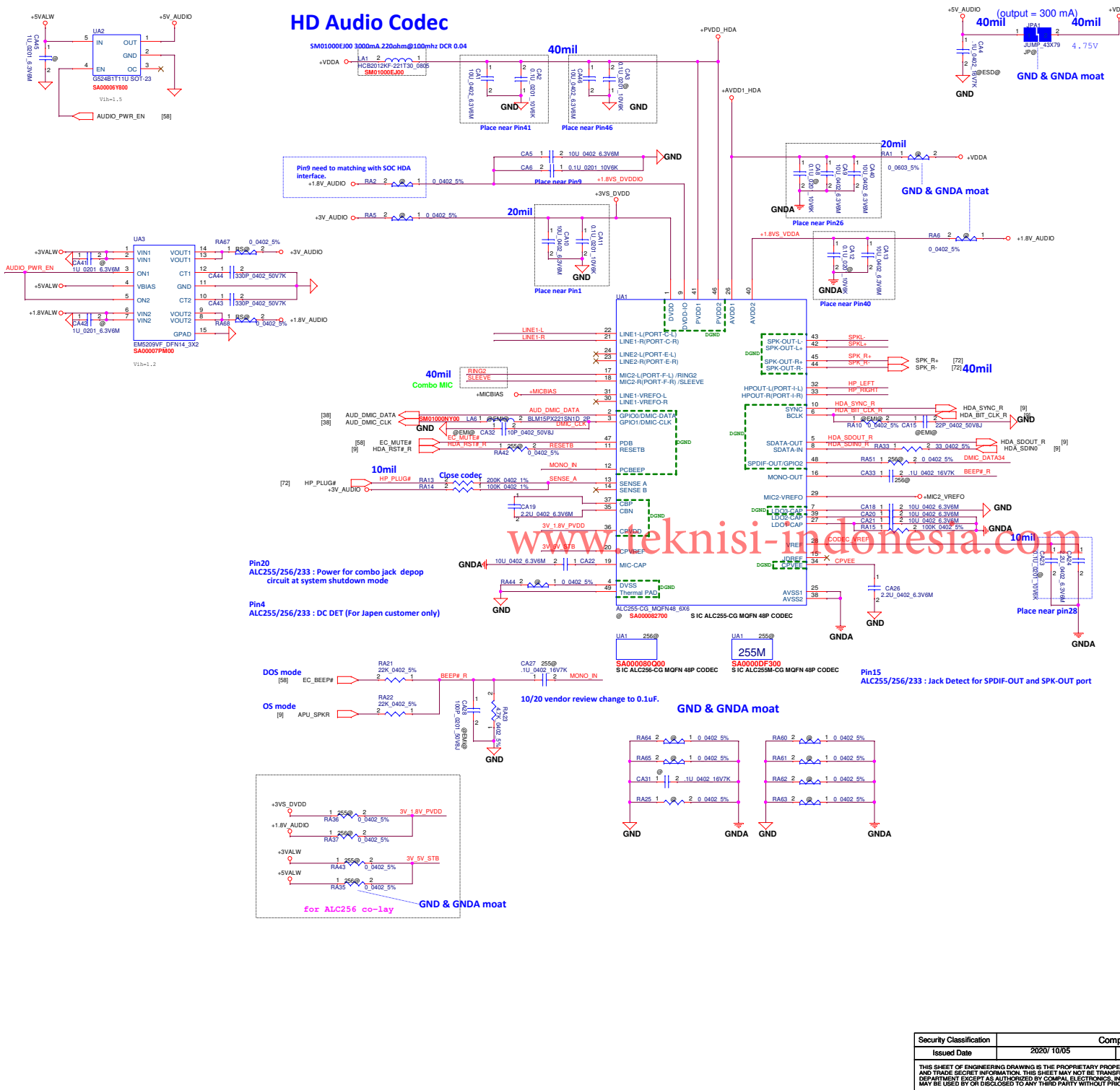
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	54 of 102
				Rev	1.0

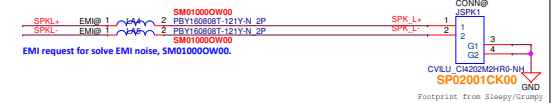
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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	55 of 102
				Rev	1.0

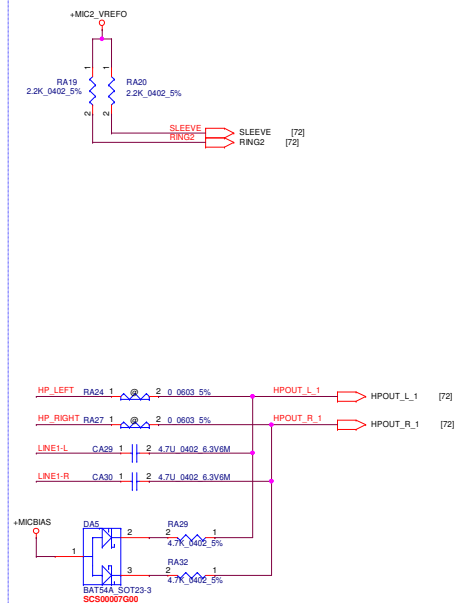
HD Audio Codec



Int. Speaker Conn.



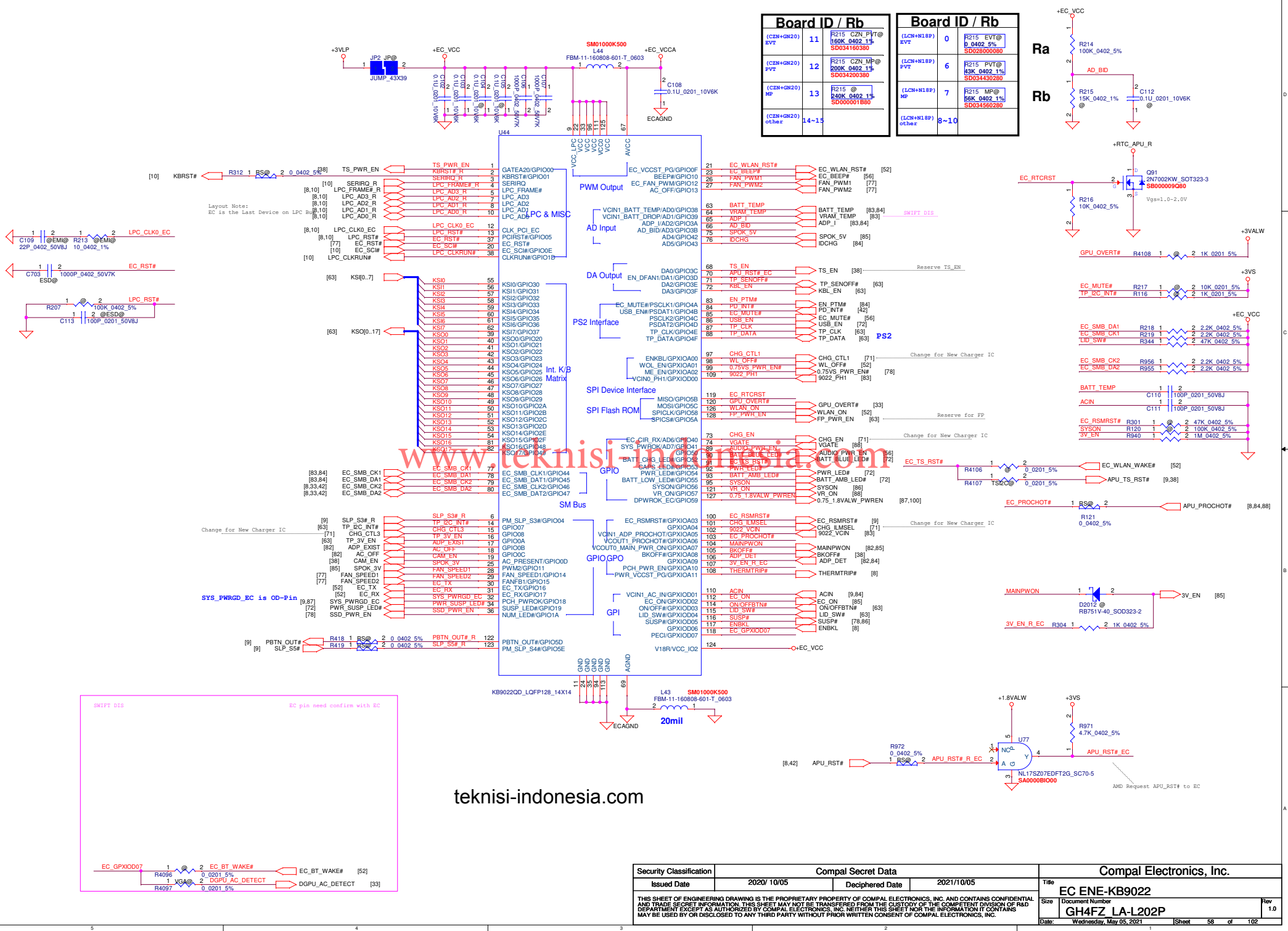
Headphone Out



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				GH4FZ	LA-L202P
				Date	Wednesday, May 05, 2021
				Sheet	56 of 102

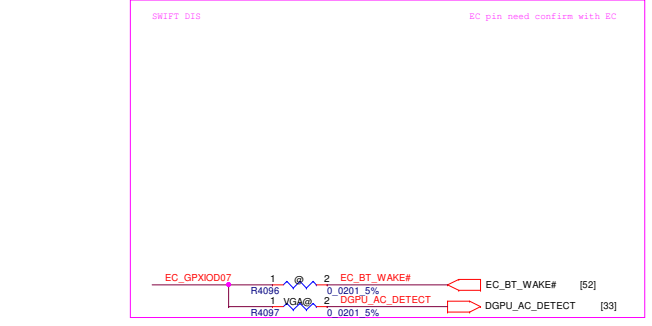
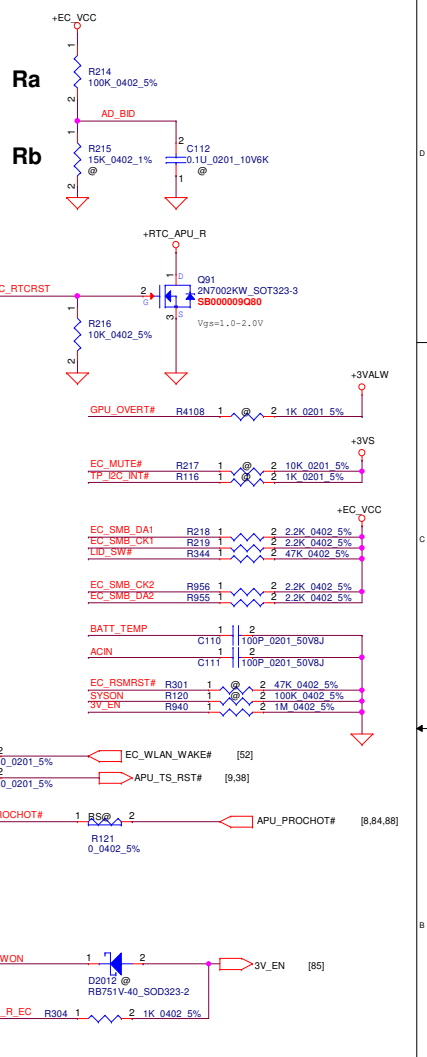
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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	57 of 102
				Rev	1.0



Board ID / Rb	
(CEN+GN20) SVT	11
(CEN+GN20) PVT	12
(CEN+GN20) MP	13
(CEN+GN20) other	14-15

Board ID / Rb	
(LCN+NL8P) SVT	0
(LCN+NL8P) PVT	6
(LCN+NL8P) MP	7
(LCN+NL8P) other	8-10



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Size		Document Number GH4FZ LA-L202P	
Date		Wednesday, May 05, 2021	
Sheet		58 of 102	

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				Custom	1.0
				Date	Wednesday, May 05, 2021
				Sheet	59 of 102

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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	60 of 102
				Rev	1.0

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Issued Date	2020/ 10/05	Deciphered Date	2021/10/05	Title	Reserve
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	61 of 102
				Rev	1.0

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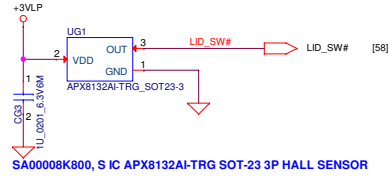
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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	62 of 102
				Rev	1.0

ON/OFF BTN

TP/B Conn.

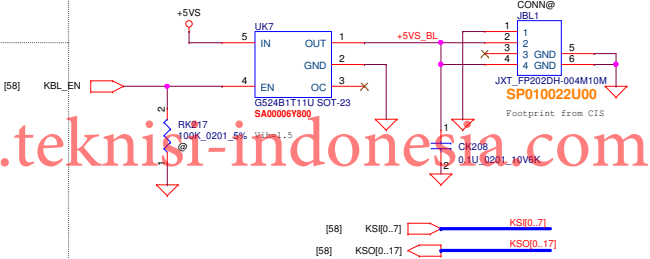


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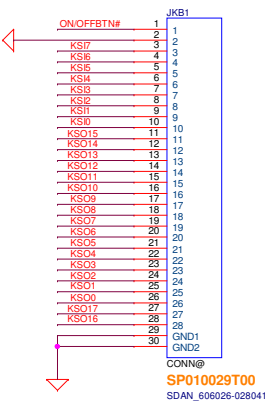
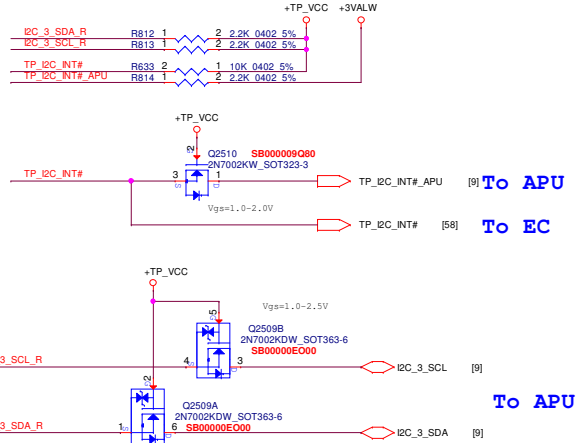
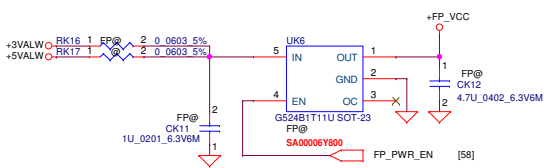
KB BackLight

KB Conn.



Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



JFP1	
PIN	SA464K-2200
1	+FP_VCC (3V)
2	D+
3	D-
4	GND
5	NC
6	NC
7	NC
8	NC

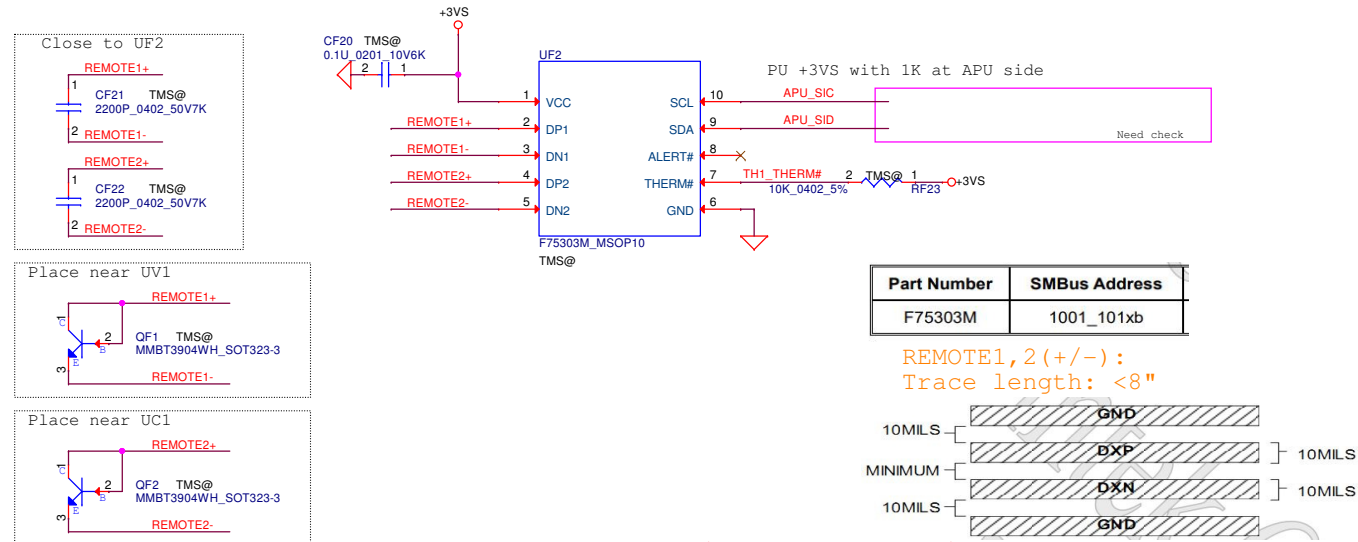
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	64 of 102
				Rev	1.0

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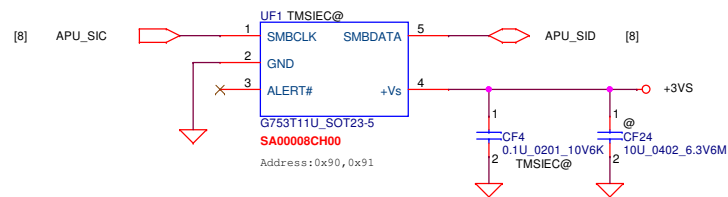
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	65 of 102
				Rev	1.0

THERMAL SENSOR (STT)



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Thermal Sensor (IEC)



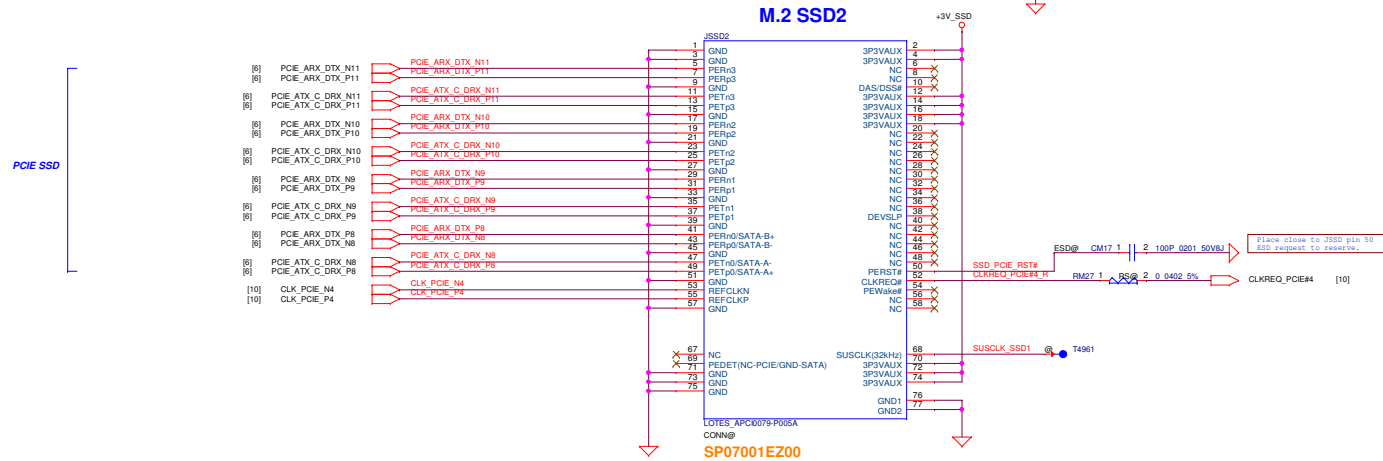
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				Date	Wednesday, May 05, 2021
				Sheet	66 of 102
				Rev	1.0
				GH4FZ LA-L202P	

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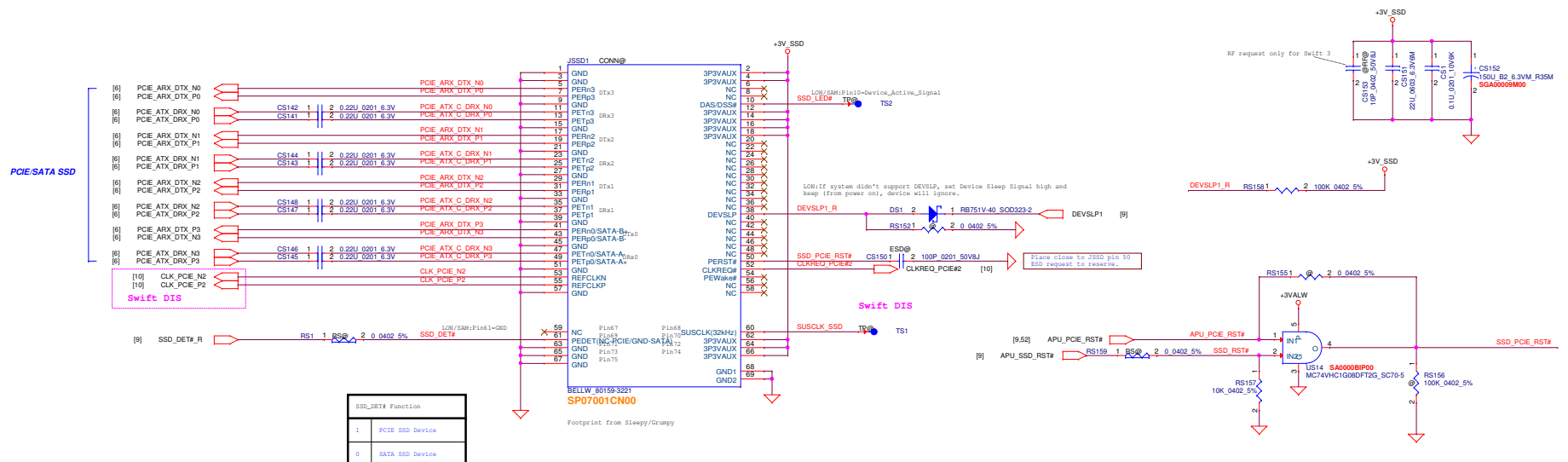
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					GH4FZ LA-L202P
				Date:	Wednesday, May 05, 2021
				Sheet	67 of 102
				Rev	1.0

M.2 PCIe SSD Conn.



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PCIE/SATA NGFF SSD Conn.



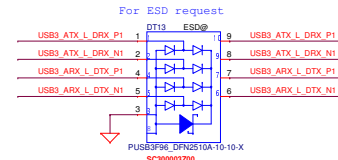
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				Sheet	69 of 102
				Rev	1.0

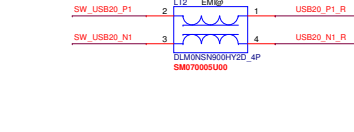
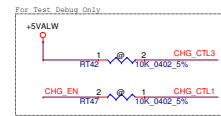
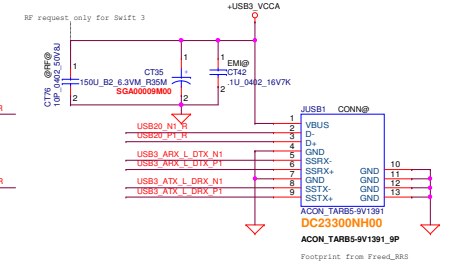
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				Sheet	70 of 102
				Rev	1.0

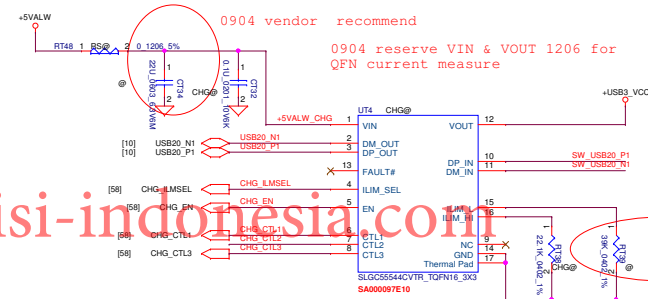
USB3.0 (Port 1)



USB3.0 Conn.



0904 vendor recommend
0904 reserve VIN & VOUT 1206 for QFN current measure



0831 Reserve ILIM_L R as vendor recommend

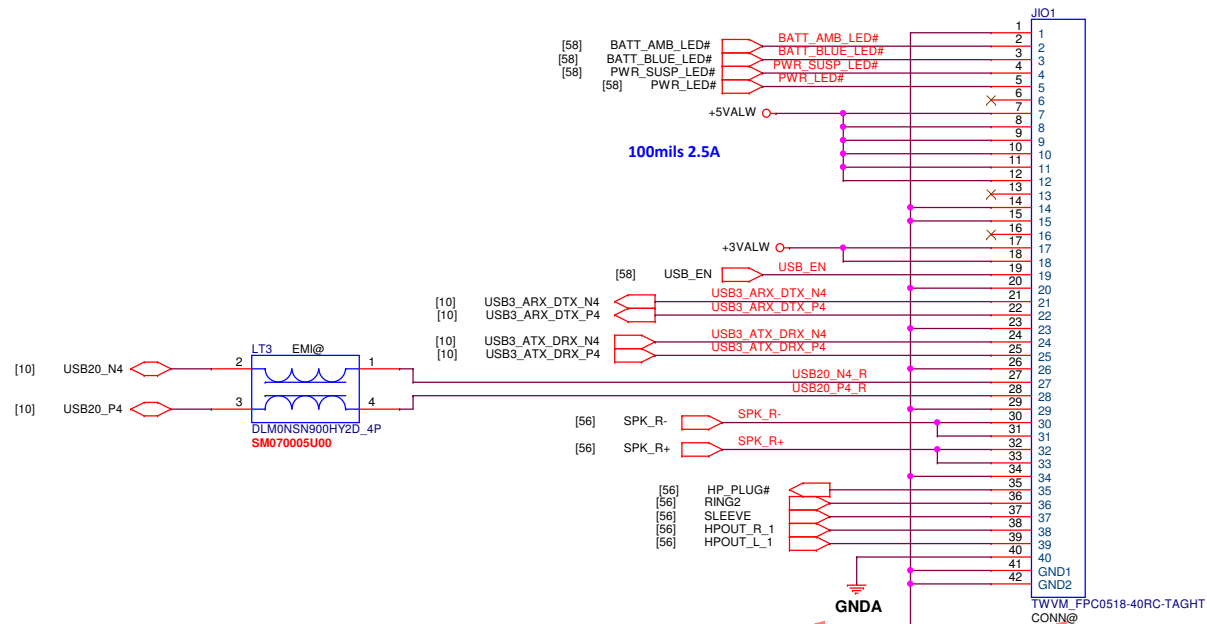
ILM R vaule
Ios (mA) =50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

IO/B



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				Date	Wednesday, May 05, 2021
				Sheet	72 of 102
				Rev	1.0
				GH4FZ LA-L202P	

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				Date:	Wednesday, May 05, 2021
				Sheet	73 of 102
				Rev	1.0

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				Sheet	74 of 102
				Rev	1.0

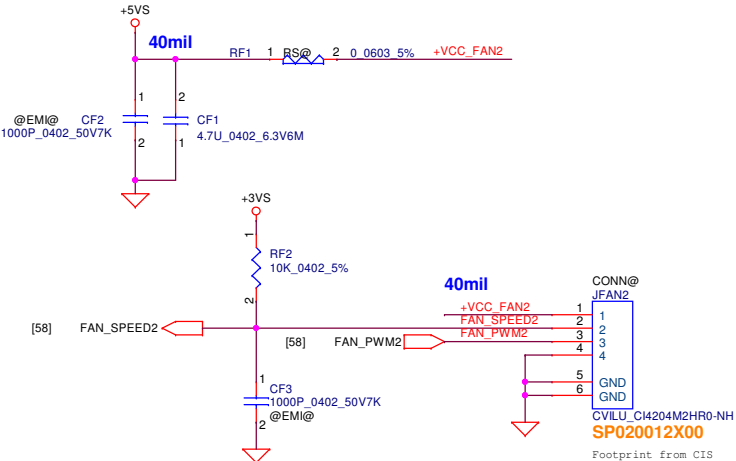
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				Date:	Wednesday, May 05, 2021
				Sheet	75 of 102
				Rev	1.0

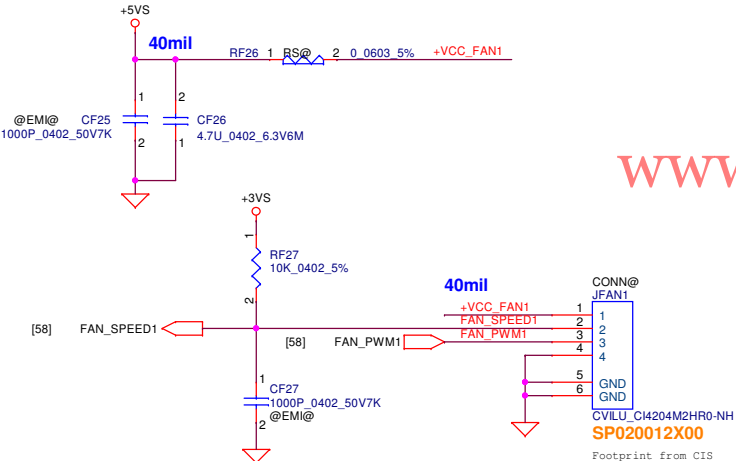
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	76 of 102
				Rev	1.0

FAN1 Conn



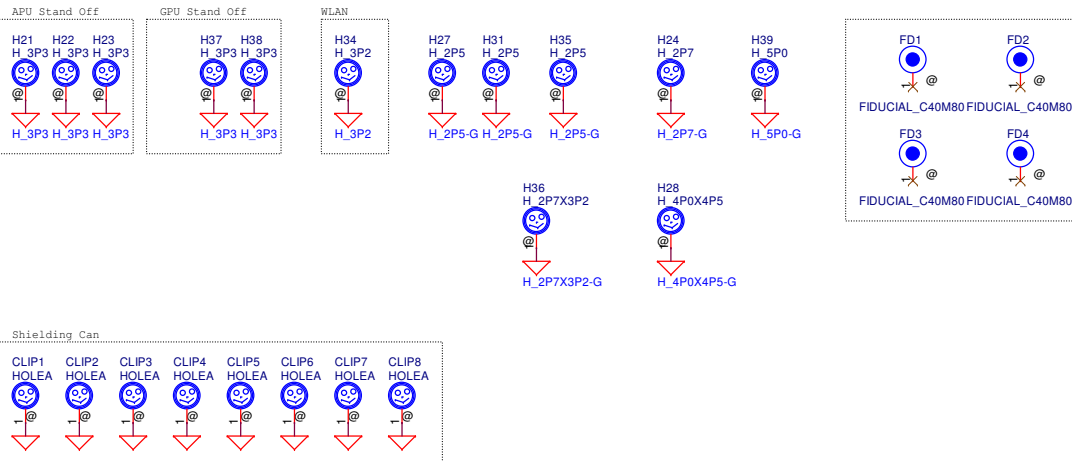
FAN2 Conn Reserve



Thermal Sensor

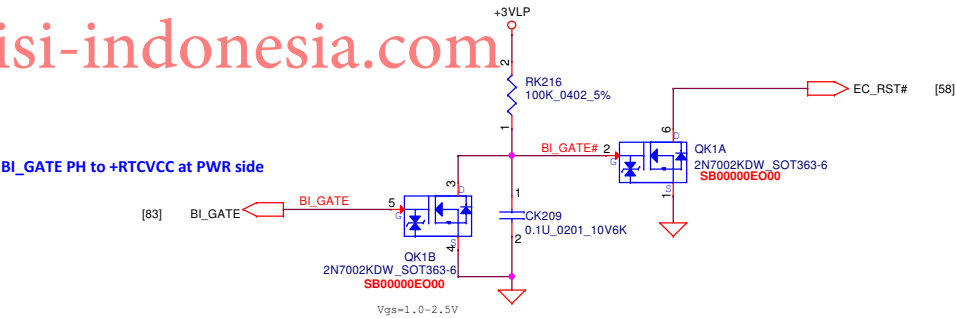
IEC thermal sensor move to page 66

Screw Hole

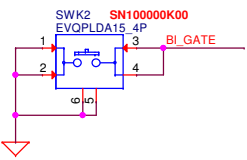


Reset Circuit

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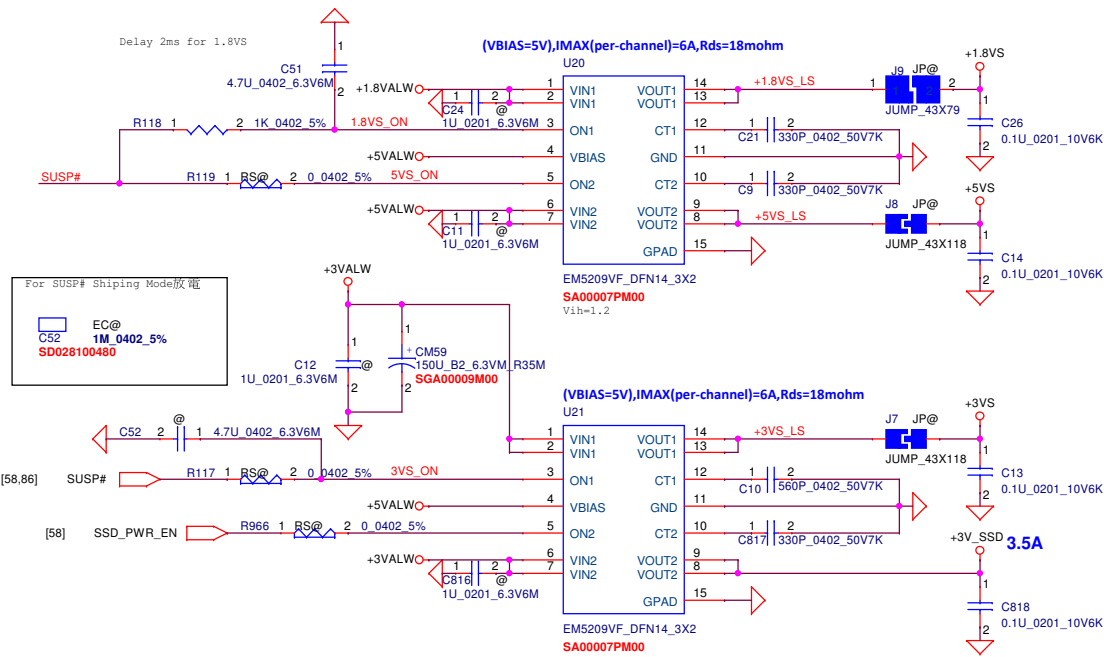


Reset Button

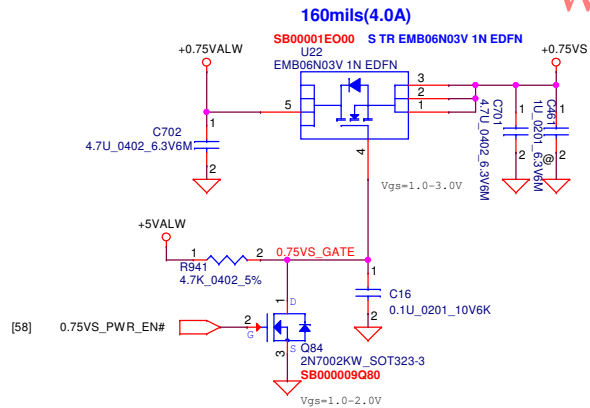


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				Date	Wednesday, May 05, 2021
				Sheet	77 of 102



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Date: Wednesday, May 05, 2021		Sheet 78 of 102			

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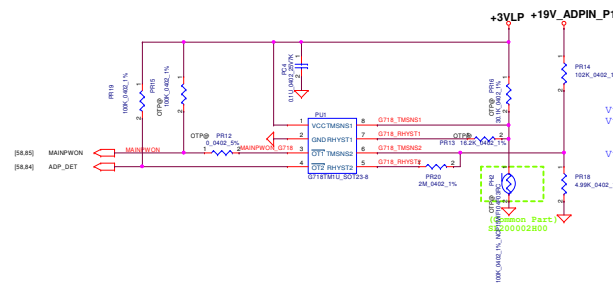
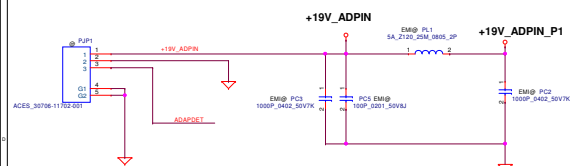
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	79 of 102
				Rev	1.0

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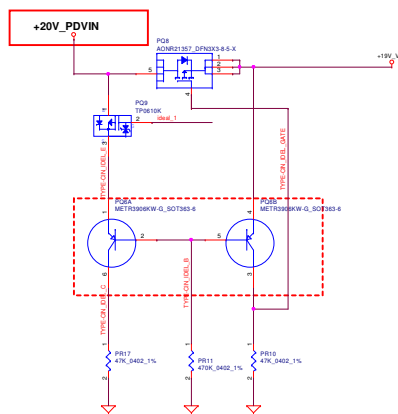
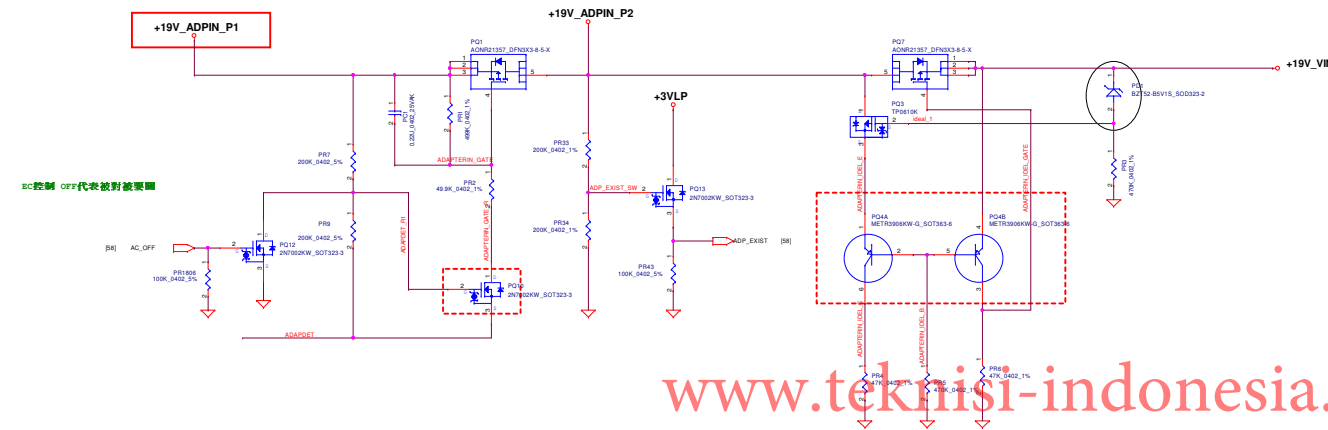
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				GH4FZ LA-L202P	
				Date:	Wednesday, May 05, 2021
				Sheet	80 of 102
				Rev	1.0

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				Date: Wednesday, May 05, 2021	Sheet 81 of 102	



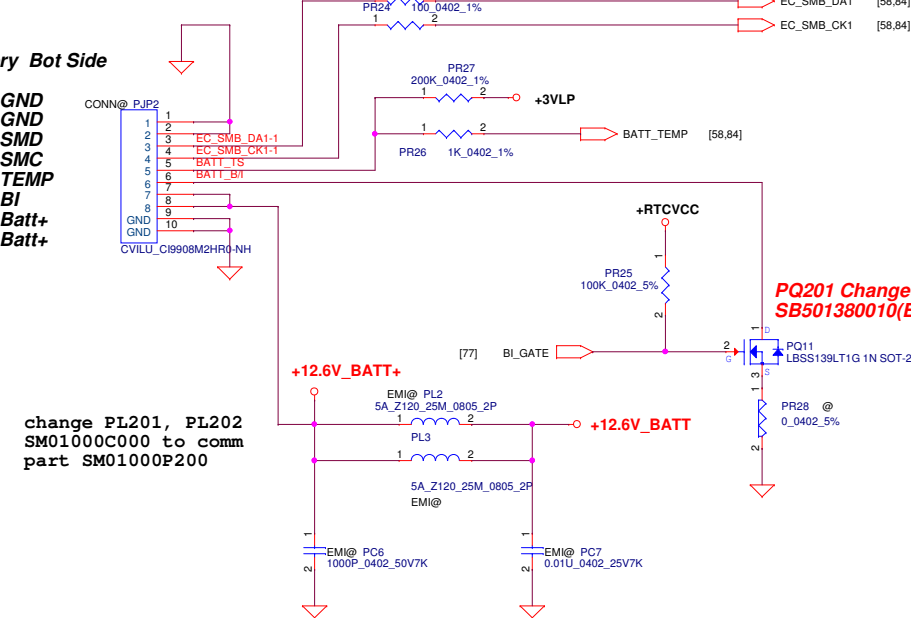
Vth=3.3/4=0.825V
Vtms=0.866V, 但因為有磁滯 RHYST2 (PR20, 2M) 電阻的影響,
當 Vcc = 3.3V時, 電壓需要超過 17.731V以上, ADP_DET (/OT2) 才會被拉 high
Vtms2>17.731V, ADP_DET拉H, 0~17.731VADP_DET拉L



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DRAWING NUMBER				GH4FZ_LA-L202P	
DATE				Wednesday, May 05, 2021	

MB:Battery Con Put TOP Side



PQ201 Change to SB00000QO00,
SB501380010(BSS138LT1G Del)

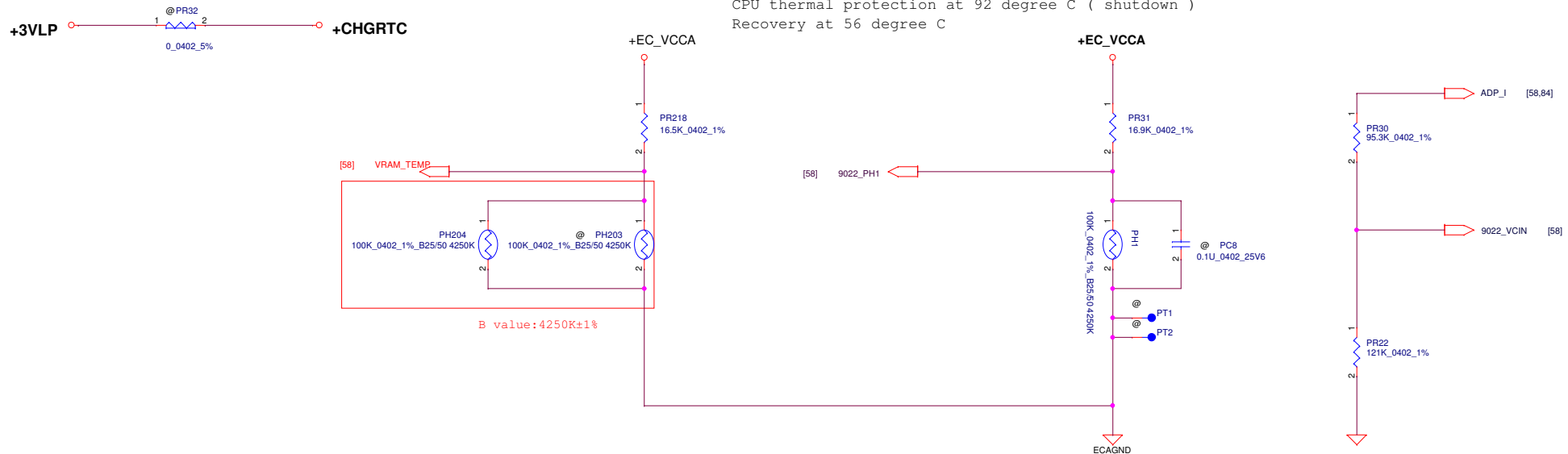
change PL201, PL202
SM01000C000 to comm
part SM01000P200

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2V

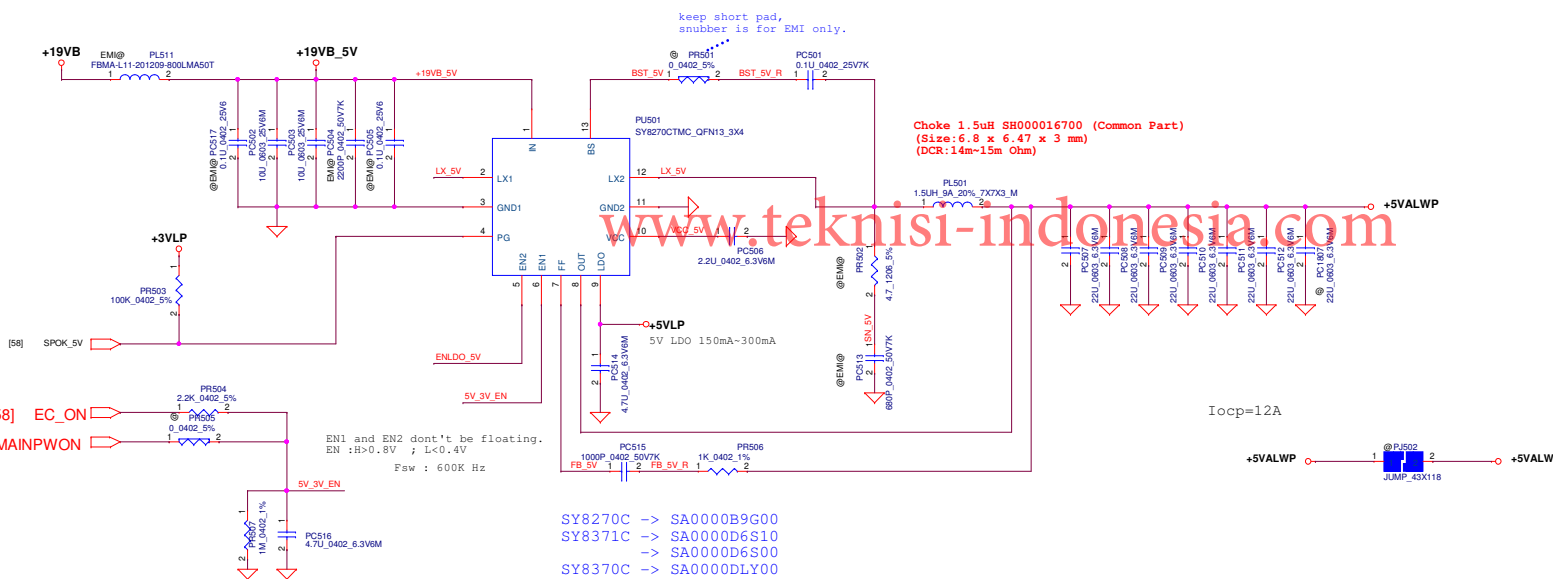
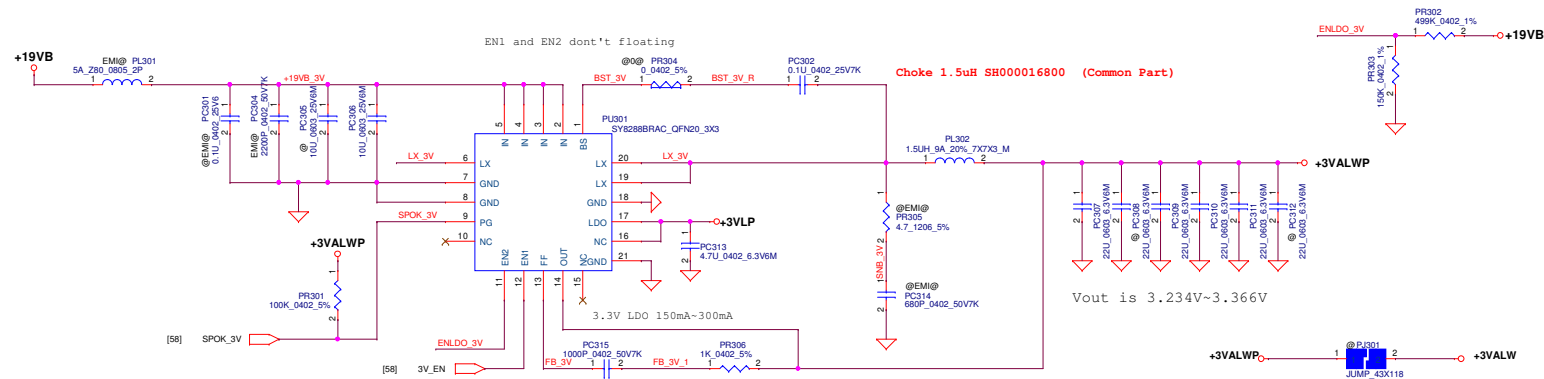
For KB9022 sense 10mΩ	Active 130% OC	Recovery
FP6 65W	84.5W, 1V	84.5W, 1V
45W	58.52W, 1V	58.52W, 1V

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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

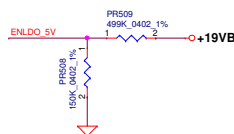


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				Rev 1.0
				Date: Wednesday, May 05, 2021
				Sheet 83 of 102



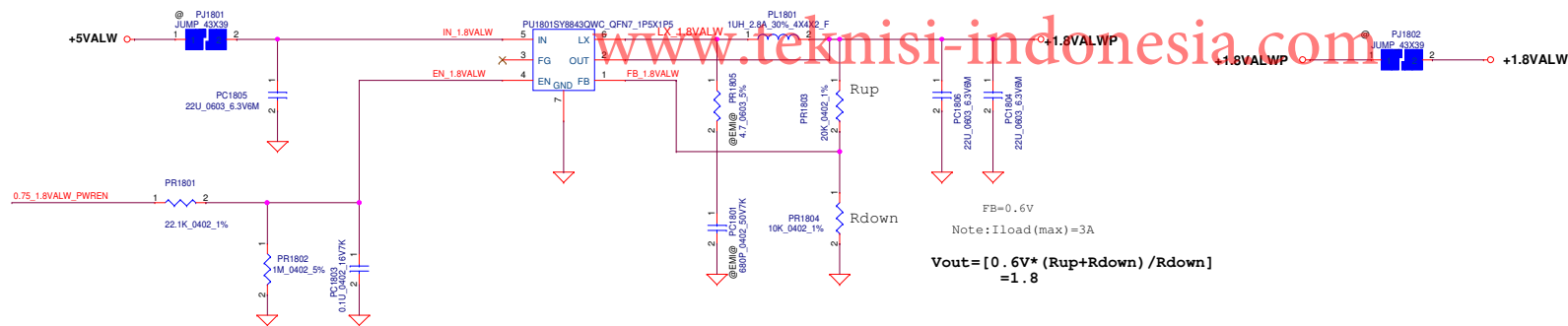
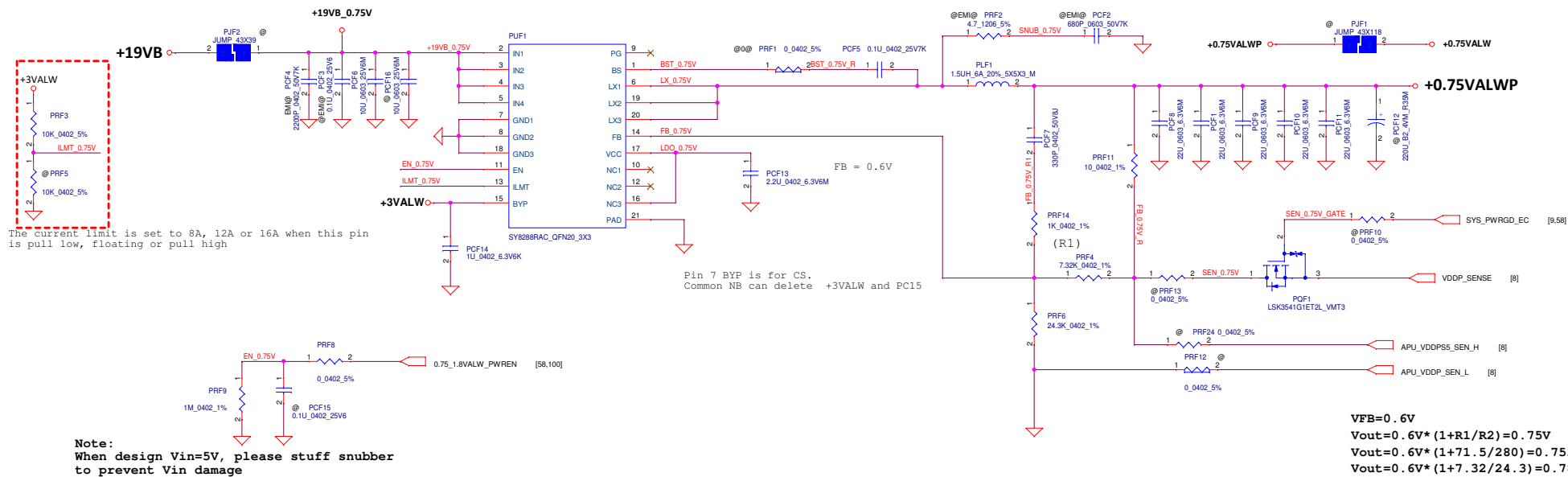
2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



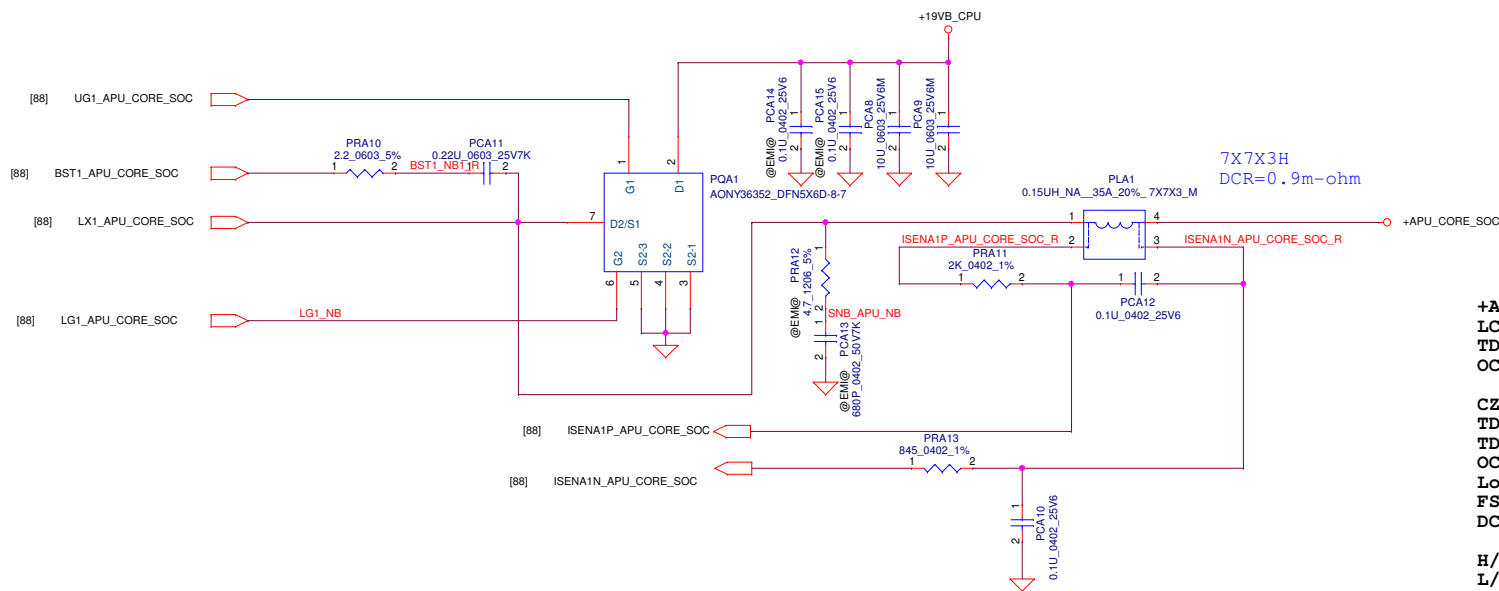
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				Custom	1.0
				Date:	Wednesday, May 05, 2021
				Sheet	85 of 102

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



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					GH4FZ LA-L202P	1.0
				Date:	Wednesday, May 05, 2021	Sheet 87 of 102



+APU_CORE_SOC
 LCN_U@15W/25W
 TDC 13A (15W/25W), EDC 17A
 OCP current ??A (35W)

CZN_U/H @25W/35W
 TDC 13A (25W), EDC 17A
 TDC 15A (35W), EDC 20A
 OCP=30A

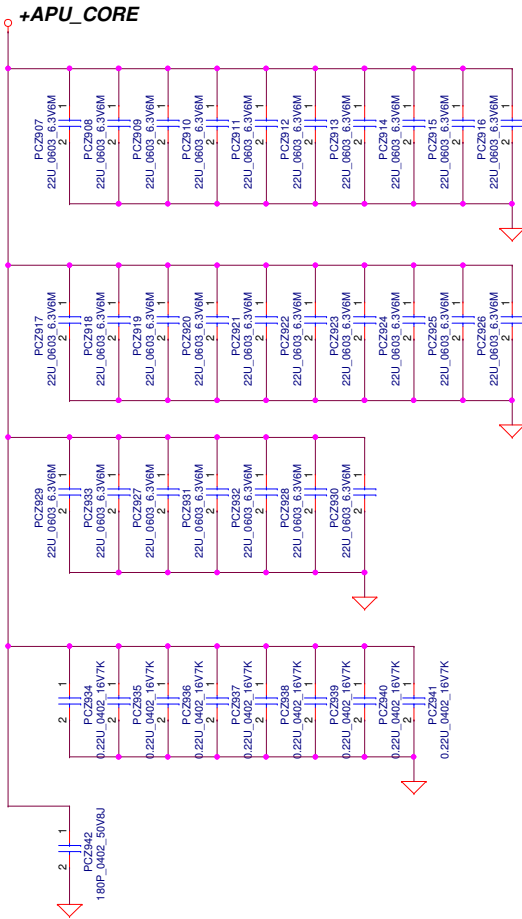
Load line -2.1mV/A
 FSW=400kHz
 DCR 0.9mohm +/-5%

TYP MAX
 H/S Rds(on) :7.3mohm , 9.1mohm
 L/S Rds(on) :2mohm , 2.5mohm

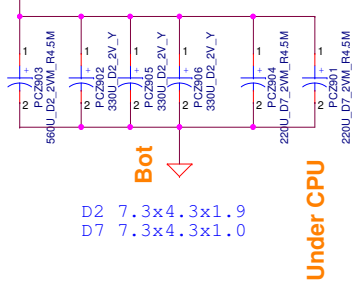
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				Rev	1.0
				Date:	Wednesday, May 05, 2021
				Sheet	90 of 102

+APU_CORE



+APU_CORE



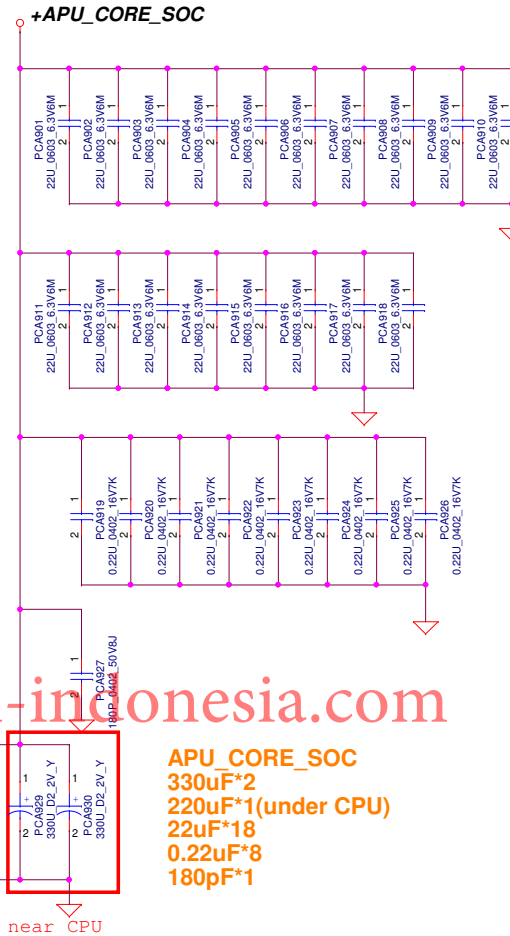
APU_CORE
 560uF*1
 330uF*3
 220uF*2(1 under CPU)
 22uF*27
 0.22uF*8
 180pF*1

330u is common part SGA00009S00

D2 7.3x4.3x1.9
 D7 7.3x4.3x1.0

Under CPU

+APU_CORE_SOC



APU_CORE_SOC
 330uF*2
 220uF*1(under CPU)
 22uF*18
 0.22uF*8
 180pF*1

near CPU

330u is common part SGA00009S00

D2 7.3x4.3x1.9
 D7 7.3x4.3x1.0

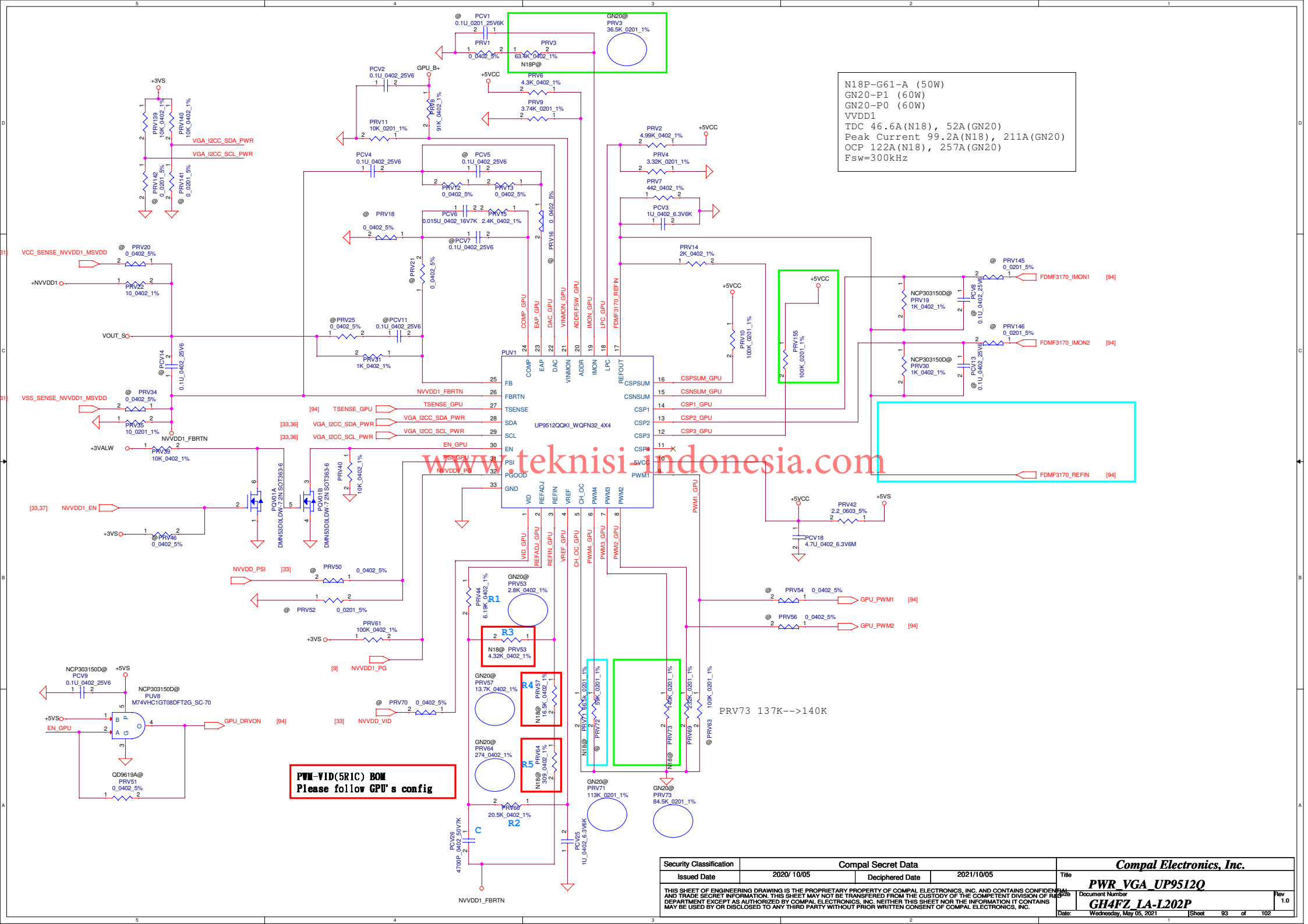
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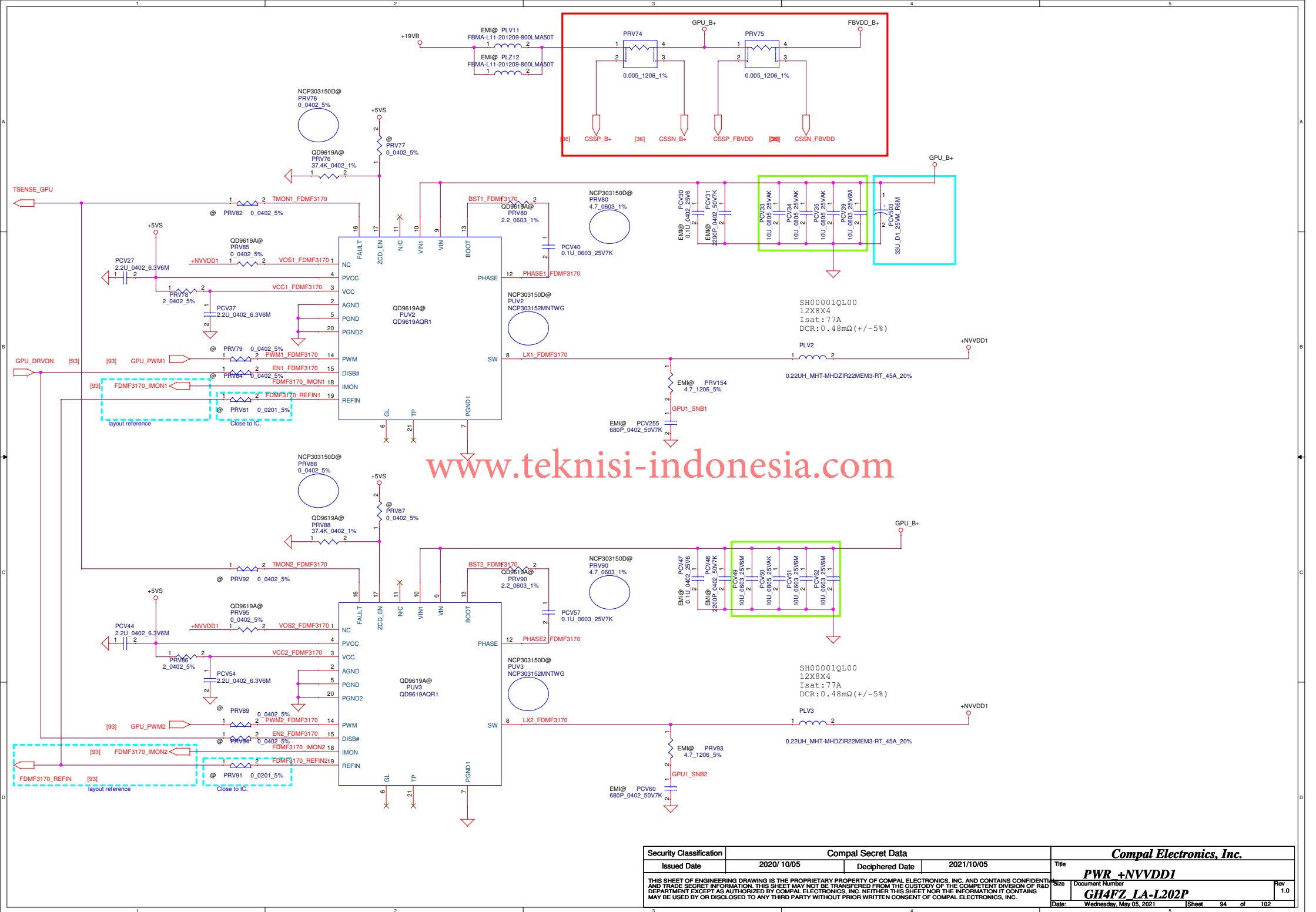
Under CPU

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Date: Wednesday, May 05, 2021					Sheet 91 of 102

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				Sheet 92 of 102	





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				Date	Wednesday, May 05, 2021
				Sheet	94 of 102
				Rev	1.0

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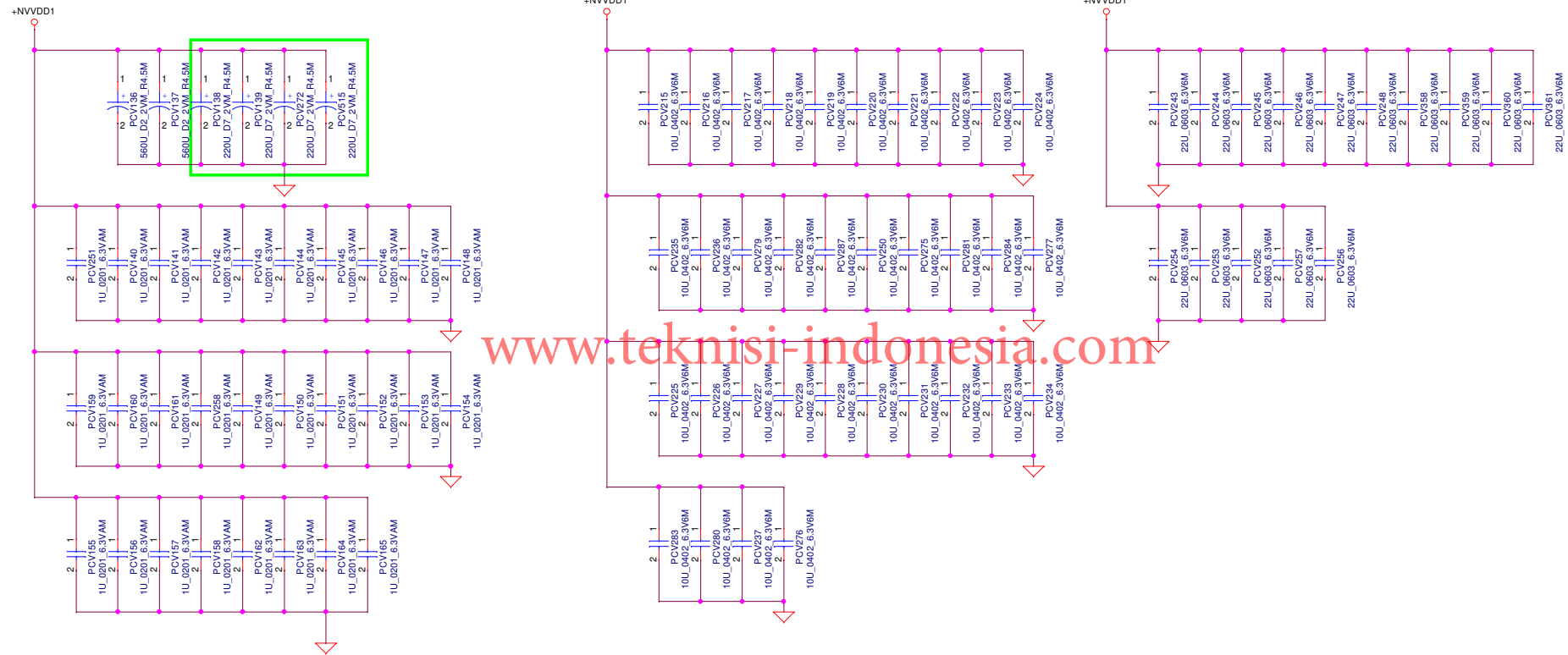
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				GH4FZ LA-L202P	1.0
				Date: Wednesday, May 05, 2021	Sheet 95 of 102

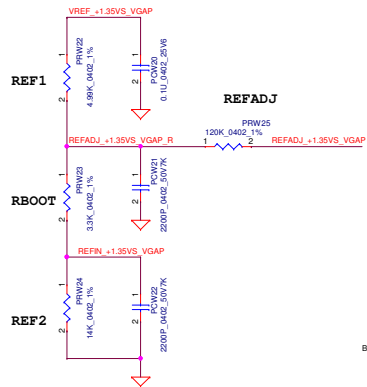
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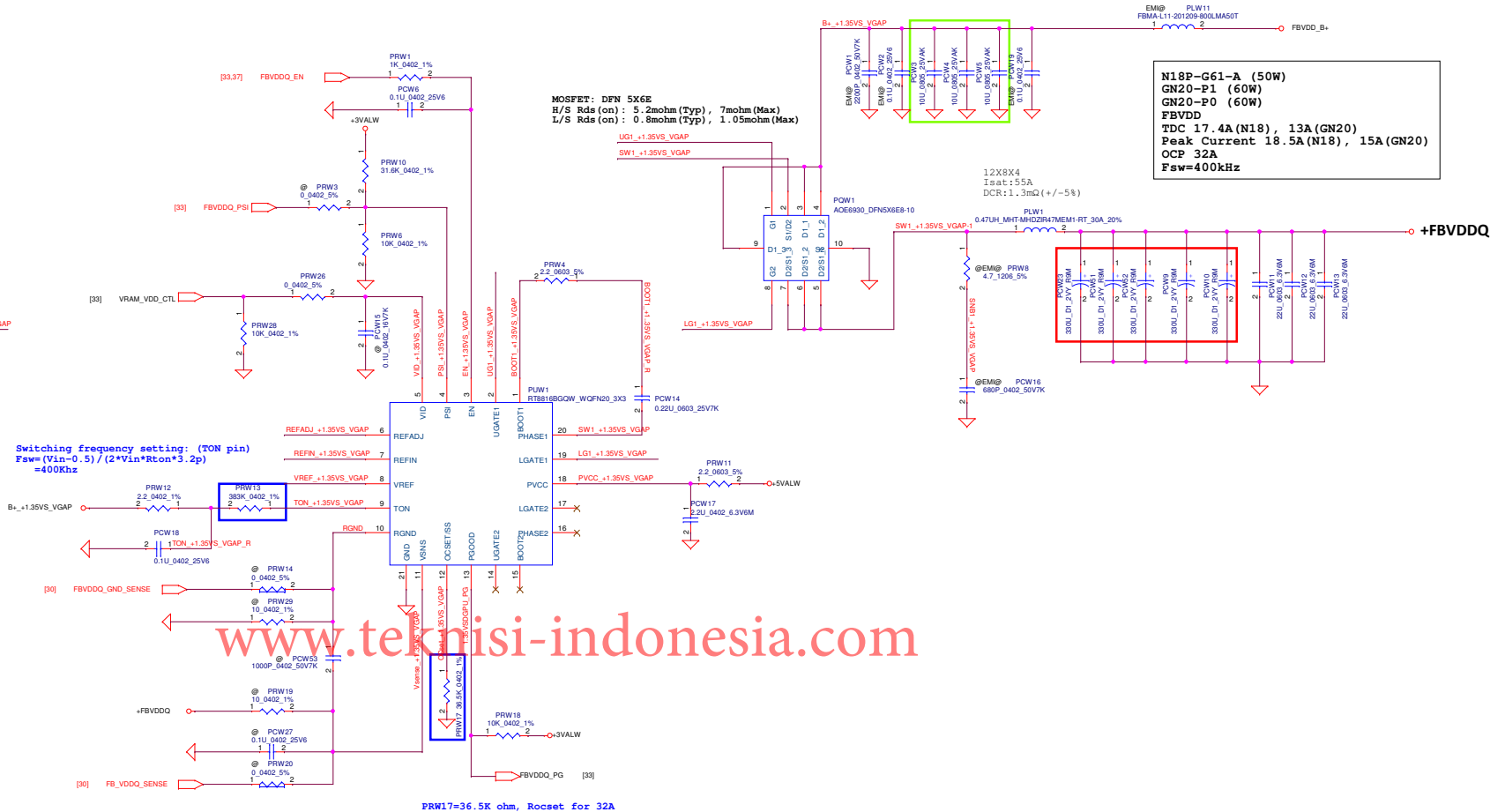
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				<i>GH4FZ_LA-L202P</i>	1.0
				Date: Wednesday, May 05, 2021	Sheet 96 of 102

+NVVDD1
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28 (13+15)





Micron & Samesung VRAM
 When, VRAM_VDD_CTL=High
 Vboot=1.25V
 When, VRAM_VDD_CTL=Low
 Vboot=1.2V
 MaxQ FBVDD P0/P3/P8 =1.2V



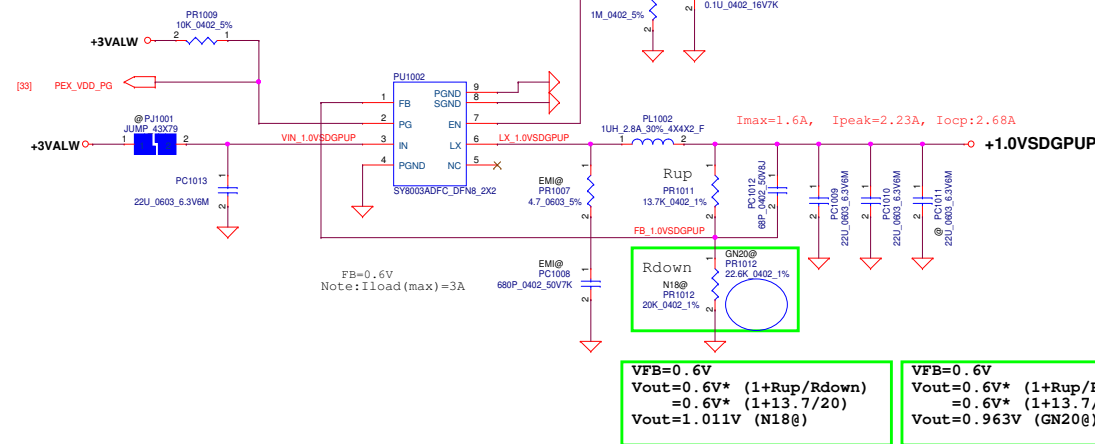
N18P-G61-A (50W)
GN20-P1 (60W)
GN20-P0 (60W)
FBVDD
TDC 17.4A (N18), 13A (GN20)
Peak Current 18.5A (N18), 15A (GN20)
OC 32A
F_{sw}=400kHz

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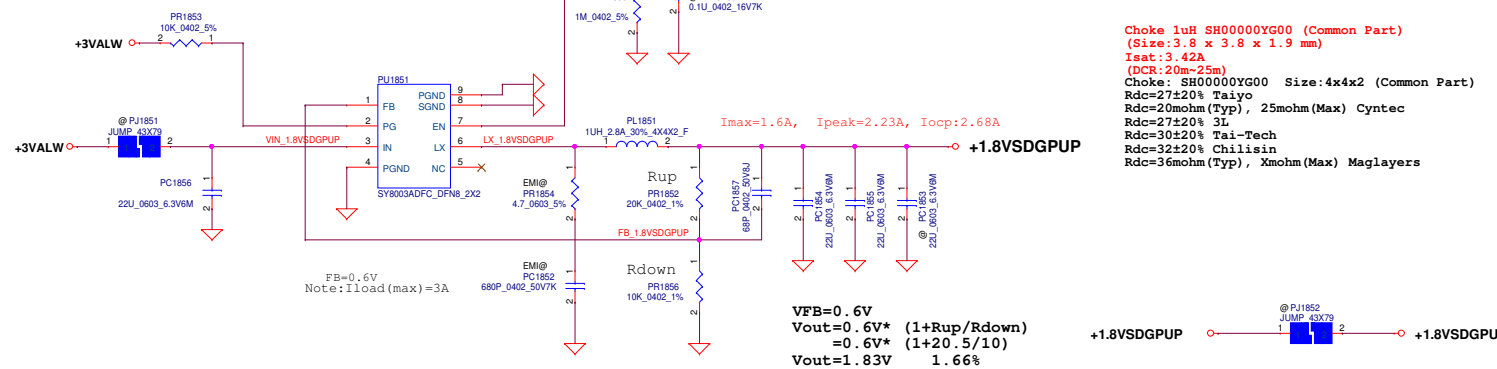
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				Date:	Wednesday, May 05, 2021	Sheet 99 of 102

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				GH4FZ_LA-L202P
				Rev 1.0
				Date: Wednesday, May 05, 2021 Sheet 100 of 102

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Issued Date	2020/ 10/05	Deciphered Date	2021/10/05	Title		
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				Custom	GH4FZ LA-L202P	1.0
				Date:	Wednesday, May 05, 2021	Sheet 101 of 102

Item	Page #	Date	Request Owner	Issue Description	Solution Description	Rev.
1		10/27	Rev0.1	schematics design finish		0.1
2		11/23		(1) Change U13,U19,U45,U8,UA2,UK6,UK7,UW1 from SA00006Y800 to SA000079400 (2) Remove R4095,no need colay (3) Add R4108 for GPU_OVERT#,Remove R973,change EGPI05C from BT_ON to GPU_OVERT#_R (4) Change R4097 to VGA@ (5) Change FAN1 & FAN2 schematics (6) Add RC839 for BIOS strap reserve (7) Change RC669,RC670 from 0402 to 0201 (8) Add test point EGPI067 (9) Add RC840,change RC729 to @ (10)Remove AGPI086,RC834,RC835 11/26 (1) Add RC840,RC841 for UMA,DIS define (2) Add RC842 for CLKREQ_PCIE#5 Add RC844 & change RC781 for EGPI070 for APU define 11/30 (1) Add RV3697,RV3698 for nVidia OVRM design change		1.0
3		01/18		(1) change UV14 from N18PA@ to @		1A
4		03/18	Change LA-L201PR1A to LA-L202PR10	(1) Add RC845 VGA@ for EGPI042 to GC6_FB_EN3V3 RC839 change to @ (2) Add RV3699 for UV15.1 +3VALW (3) Change OVRM VCC to +3VALW,RV178 to +3VALW (4) Change GPU_OVERT# to PU +3VALW Change RV4108 to @ (5) Change RV167.2 to +5VALW (6) Add RK217 to @	LA-L202P Rev:1.0	

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Custom	GH4FZ LA-L202P	1. A	1.0	
Date	Wednesday, May 05 2021	Sheet	102	102